

*Applications of signal processors*

# *INTERFACES OF SIGNAL PROCESSORS*

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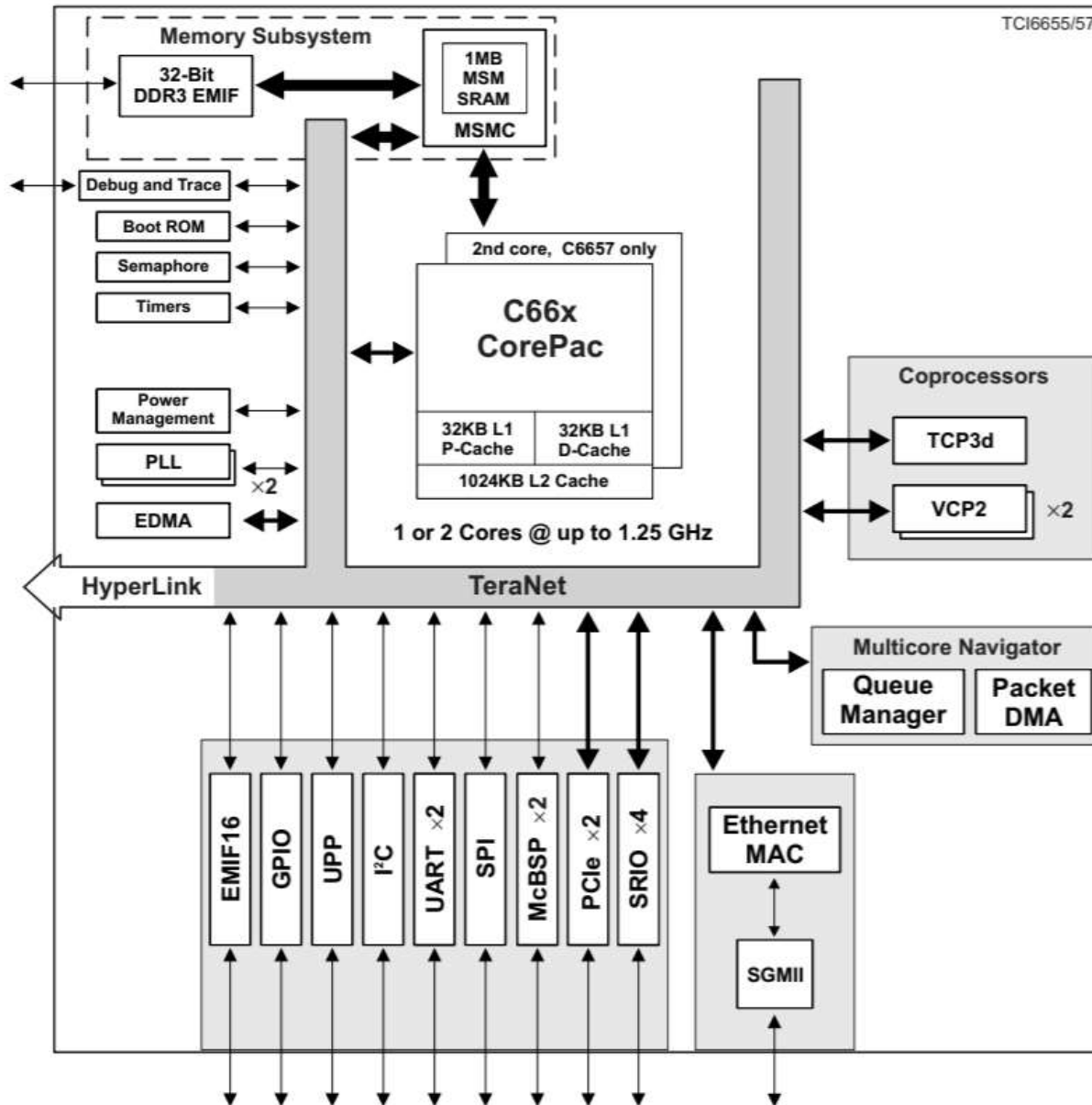
# Interfaces of digital signal processors

- A signal processor must get data from the inputs and pass the processing results to the outputs
- Interfaces are used for acquisition and transfer of signals in different formats.
- Interfaces are available at the DSP chipset pins.
- The number of interfaces and their types depend on the DSP model.



1	VDD	SP14	SP16	TRST	SSA_CLK GPIV, SP14	SSA_DIN SSA_CLK GSE2	SSA_DQ GPIV	SP17	SSA_DQ GPIV, SP17	SSA_DIN SSA_CLK GPIV	SSA_DQ GPIV, SP17	SSA1_CLK GPIV, SP17	SSA1_DQ GPIV, SP17	SSA1_CLK GPIV, SP17	SSA1_DQ GPIV, SP17
2	VDD	SP12	SSA	SP18	SP19	SSA	SP19	SP19	SP19	SSA1_CLK GPIV, SP19	SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19
3	SSA1	SP13	SP19	SP19	SP13	SP19	SSA1_CLK GPIV, SP19	SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19
4	SP13	SSA1	SP13	SP19	SSA	SSA	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19
5	SP13	SSA	SSA	SSA	SSA	SSA	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19
6	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19
7	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19
8	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19
9	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19
10	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19
11	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19
12	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19
13	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19
14	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19
15	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19
16	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19	SSA1_CLK GPIV, SP19	SSA1_DQ GPIV, SP19

# Interfaces of TI C6657 DSP



# *Digital serial interfaces*

- In serial interfaces, bits of a digital signal are transmitted in serial, one by one.
- The majority of DSP interfaces are serial ones.
- Serial interfaces may be:
  - **synchronous** – data and clock; pulses of the clock signal determine where each bit starts,
  - **asynchronous** – data only, the clock signal must be generated by the receiver, so the transmission rate must be known.

# UART (RS232, RS485)

UART – *Universal Asynchronous Receiver/Transmitter*

- Asynchronous interface.
- Relatively low speed (in practice: max. 115200 b/s).
- Transmission: start bit, 5-9 data bits (usually 8 bits), parity bit (optional), 1-2 stop bits.
- The receiver must know the data format. Example specification: **9600/8N1** – speed 9600 bit/s, 8 data bits, no parity bit, one stop bit (this is the standard).
- Used mainly for communicating with external devices.
- Data exchange often requires special protocols, e.g. MODBUS.

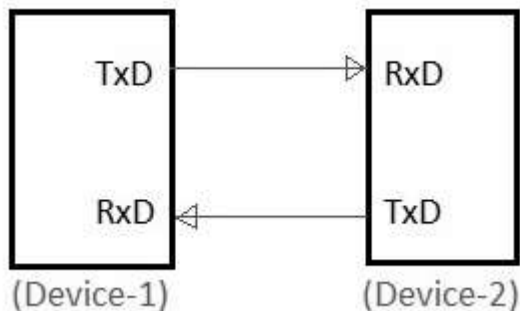
# UART (RS232, RS485)

Connections:

- Tx (*transmit*) – for sending data,
- Rx (*receive*) – for getting data,
- power supply (VCC) and ground (GND) lines.

WARNING: lines are “crossed” when connecting devices:

Rx1 – Tx2, Rx2 – Tx1



# I<sup>2</sup>C

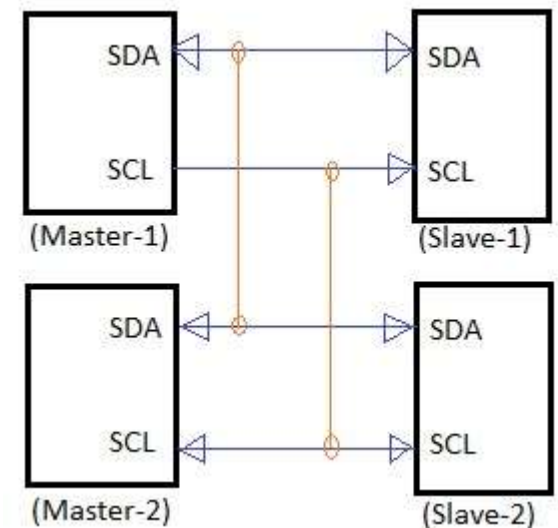
## I<sup>2</sup>C – *Inter-Integrated-Circuit*

- Standard in communication with various digital sensors.
- Synchronous interface. Data line (SDA) and clock line (SCL).
- A DSP is the transmission manager (*Master*).
- Multiple external devices (*Slave*) may be connected.
- Each slave must have a unique address.
- Maximum speed: 100 kbit/s (*Standard*), 400 kbit/s (*Fast*), there are extensions to 3.4 Mbit/s.
- Transmission speed depends on the length and quality of the connection wires and on the number of connected devices.

# I<sup>2</sup>C

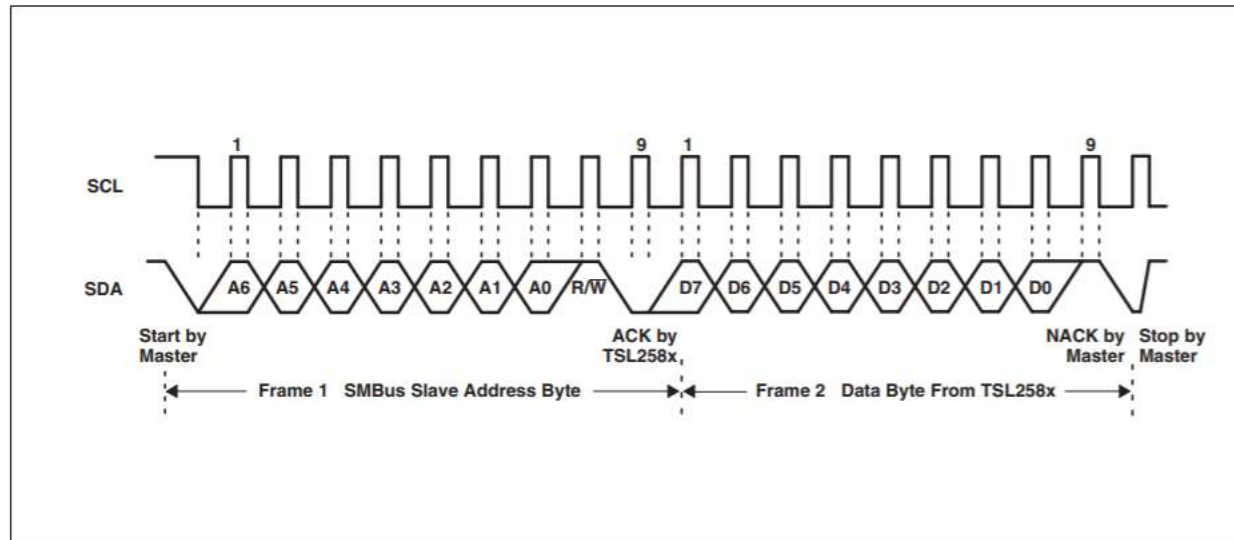
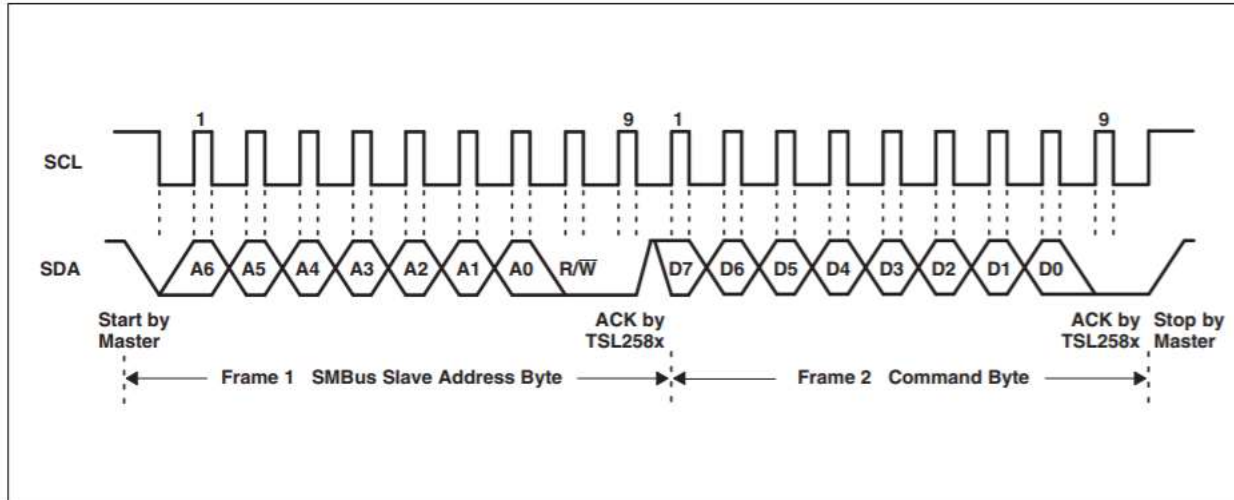
A simplified description of transmission:

- The master switches the SDA and SCL state, sends the target address to all connected devices.
- A slave having the required address responds with ACK and switches the SDA line.
- Data transmission is performed via SDA.
- The receiver responds with ACK.
- The master closes the transmission by switching the SCL and SDA lines.





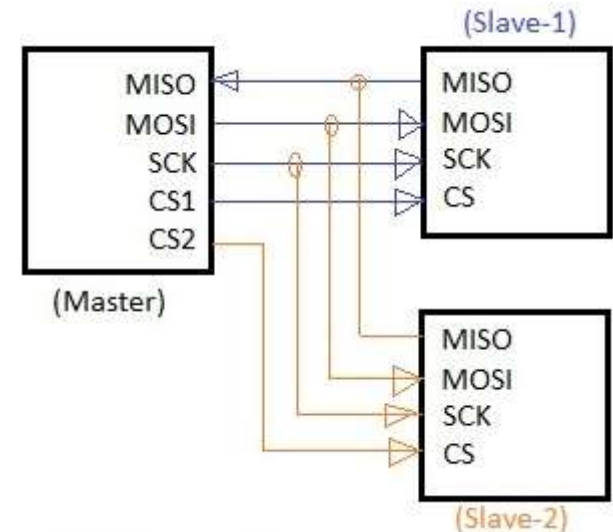
# I<sup>2</sup>C - a transmission example



# SPI

## SPI – *Serial Peripheral Interface*

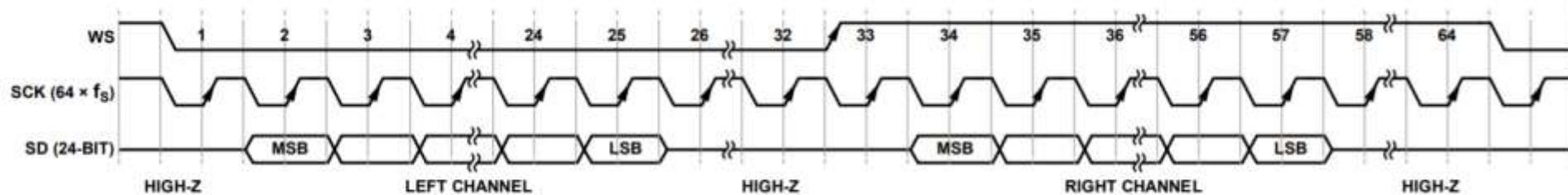
- Synchronous interface.
- Multiple devices may be connected to one Master, but each device requires its own *Chip Select (CS)* line.
- 4 lines: MOSI (*Master Out, Slave In*), MISO (*Master In, Slave Out*), CLK (clock signal), CS (chip select).
- Much higher speeds than I<sup>2</sup>C, about 8 Mbit/s.
- Fully bi-directional communication (*full duplex*).
- Used when high transmission speed is required, e.g. memory cards, displays.



# I<sup>2</sup>S

I<sup>2</sup>S – *Inter-IC Sound* (do not confuse with I<sup>2</sup>C)

- Used for transmission of digital sound samples.
- Lines:
  - SCK – clock signal, pulse for each bit,
  - WS (FS) – word (frame) clock signal, changes state for the first bit of each sound sample (0/1 for L/R channel).
  - SD – data line, bits of the digital sound.
  - MC – master clock, optional synchronizing clock.



# USB

## USB – *Universal Serial Bus*

- Allows a DSP to communicate with USB peripherals:
  - DSP as *USB Slave* – read/write data from an external device,
  - DSP as *USB Master* – other devices may connect to the DSP and get data, e.g. the processing results.
- Rarely used in DSPs for signal transmission, often used in a “diagnostic mode”.
- Transmission speed depends on the standard (1.0: 1.5 Mb/s; 1.1: 12 Mb/s, 2.0: 480 Mb/s).

# GPIO

## GPIO – *General Purpose Input and Output*

- Digital interface with unspecified function or format. A programmer can write/read any signal.
- Good for bi-state signals (“on-off”), e.g.:
  - reading button state (0 – pressed, 1 – released),
  - controlling LED diode (1 – light, 0 – turn off).
- Any signals can be transmitted but reading and writing signals (“bit banging”) must be performed by a programmer and it is less efficient than standard interfaces.

# GPIO

- Each GPIO pin can be configured as input or output.
- The default state of GPIO line is undefined (floating) and it can change by itself.
- The default state (0 or 1) must be configured with an internal resistor:
  - *pull-up* – set the default state as high (1),
  - *pull-down* – set the default state as low (0).

<https://www.freecodecamp.org/news/a-simple-explanation-of-pull-down-and-pull-up-resistors-660b308f116a/>

# Network interface

## *Ethernet, EMAC (Ethernet Media Access Controller)*

- Allows a DSP to function as a networked device.
- Requires a network stack implementation in software (e.g. TI NDK – *Network Development Kit*).
- Transmission speed depends on the type.  
GbE (*Gigabit Ethernet*) – up to 1 Gb/s.
- Implemented mainly in the modern floating-point DSPs.
- A convenient method of transmitting any digital signal, e.g. sound samples.

## *Parallel digital interfaces*

- Contrary to serial interfaces, in the parallel interface, all bits are available at the same time at the input/output.
- Requires a separate data line for each bit.
- Relatively rare in DSPs.
- Higher transmission speed than in serial interfaces.
- Useful for communication with devices requiring high data rate, such as analog to digital converters.
- Example: uPP (*Universal Parallel Port*) in TI C6657, 8 to 16 bits.



# Analog interfaces

- Processing analog signals by DSP requires an ADC – analog to digital converter.
- ADCs may be:
  - embedded in DSP (e.g. SAR – *Successive Approximation Register*),
  - external – communicating e.g. through SPI or I<sup>2</sup>C.
- Parameters:
  - speed, in samples per second (sa/s),
  - bit resolution (e.g. 8, 12, 16 bit).
- SAR ADC in C5535: 10 bit, up to 64 ksa/s.

# *External memory interfaces*

Communication between DSP and the external memory:

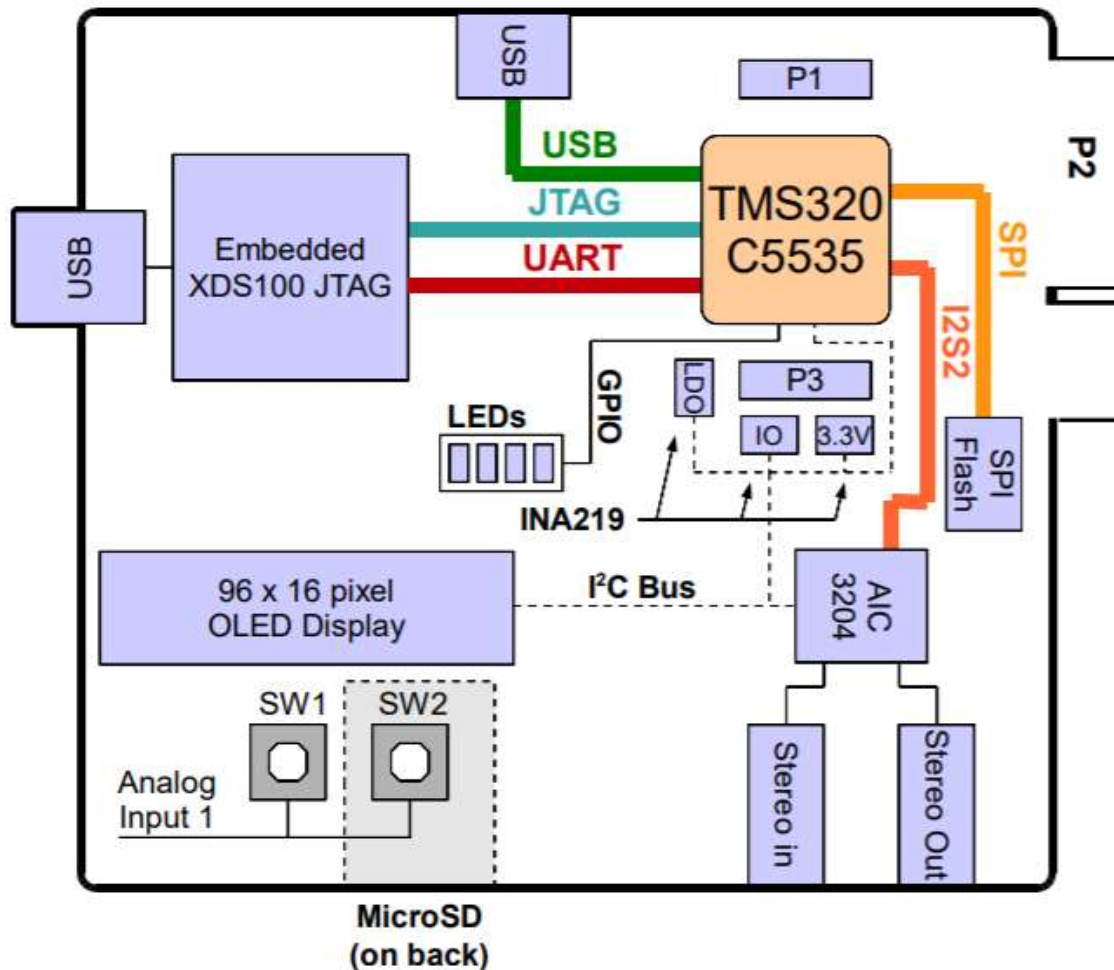
- DDR – additional DDR3 memory chipsets,
- eMMC/SD – communication with Flash memory cards,
- EMIF (*External Memory Interface*) – a unified interface for communication with external memory of different type (Flash, SRAM, SDRAM).

## *Other interfaces*

- *PCI Express (PCIe)* – for communication with devices working in this standard; high speed.
- *HyperLink* – used for connecting multiple DSPs from Texas Instruments and data exchange.
- *McBSP (Multichannel Buffered Serial Port)* – interface from Texas Instruments, a multichannel serial interface used mainly for sound signals.
- *SRIO (Serial RapidIO)* – a high speed serial interface.

# Example of using interfaces in DSP

C5535 DSP and the development board (used in the course project)



# *Development board eZdsp5535*

- Flash memory 8 MB (SPI interface)
- Alphanumeric OLED display, 96×16 px (I<sup>2</sup>C)
- 5 LEDs (GPIO)
- 2 buttons (GPIO, analog inputs through SAR ADC)
- ADC and DAC – AIC 3204 sound codec (I<sup>2</sup>S)
- USB 2.0
- Debugging interfaces (JTAG, UART)
- Voltage probes (I<sup>2</sup>C)
- Interfaces available on the board connectors