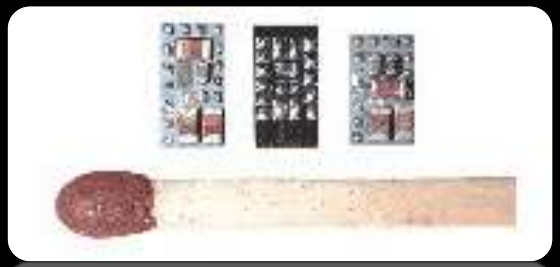
Apllications of signal processors

Piotr Odya
pioodya@pg.edu.pl
Department of Multimedia Systems

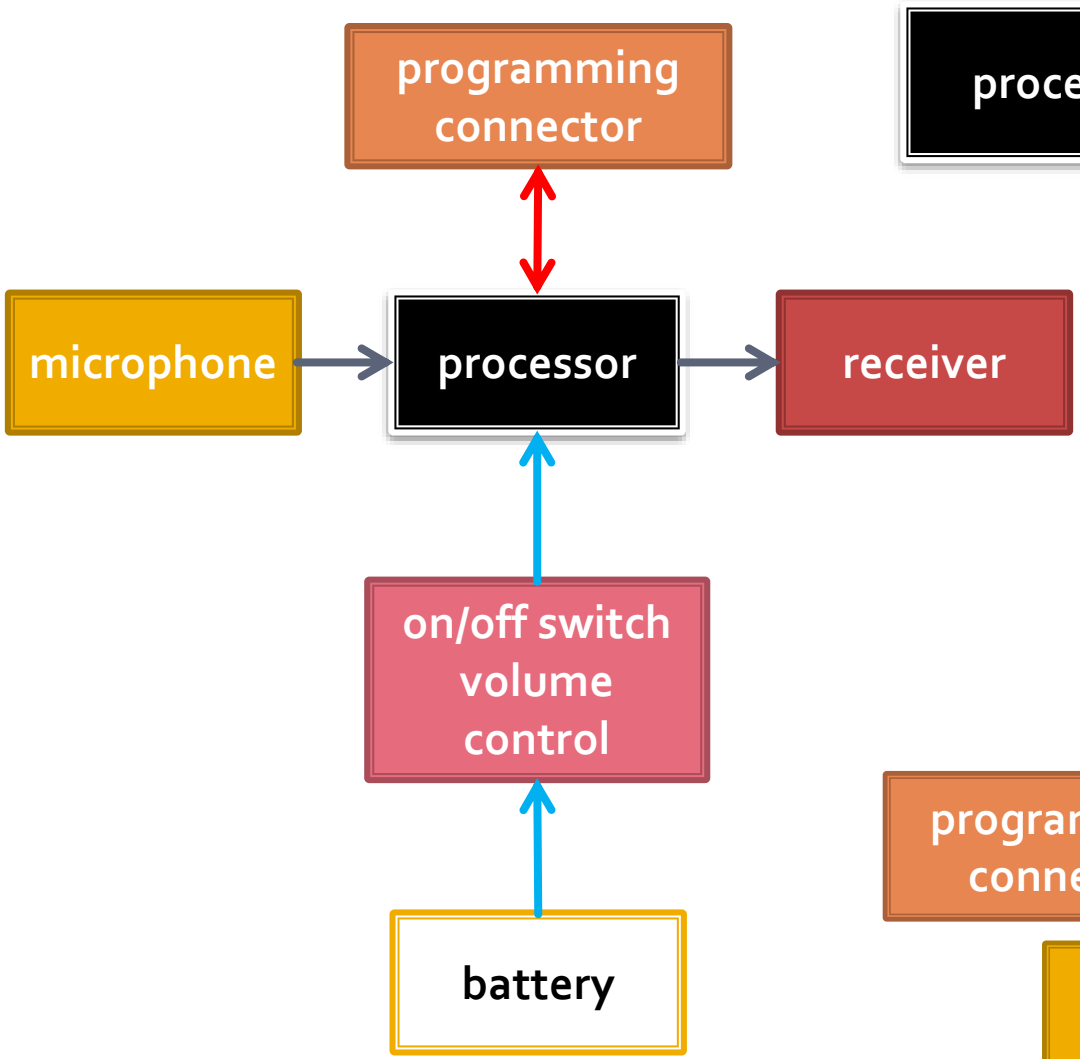
Signal processors in hearing aids (but not only)

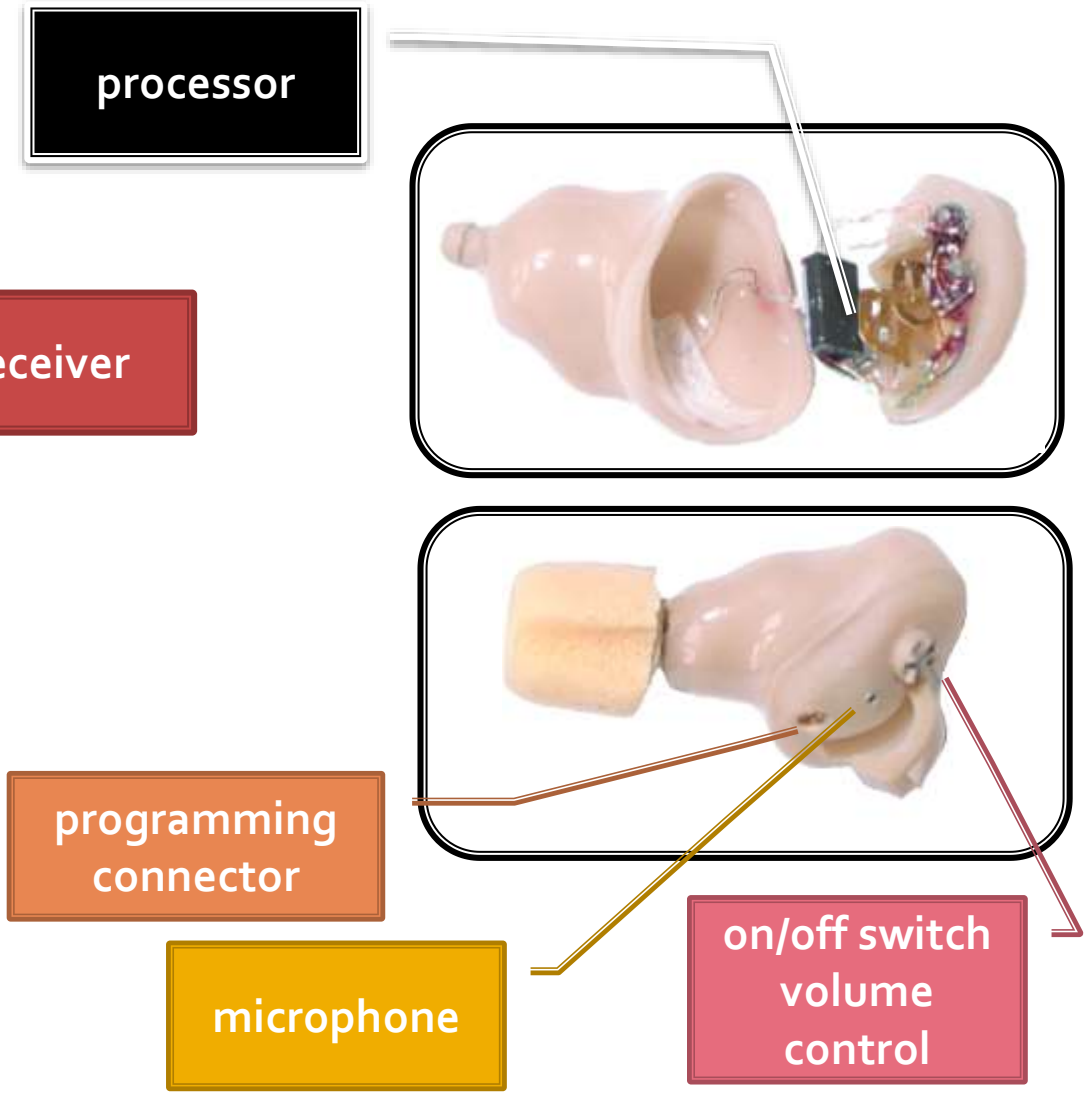
Introduction



- typical use: hearing aids
  - typical construction
- small dimensions
  - the device must fit in the ear canal
- low power consumption
  - the device should work for many hours
- easy programming of device parameters

Hearing aid - construction





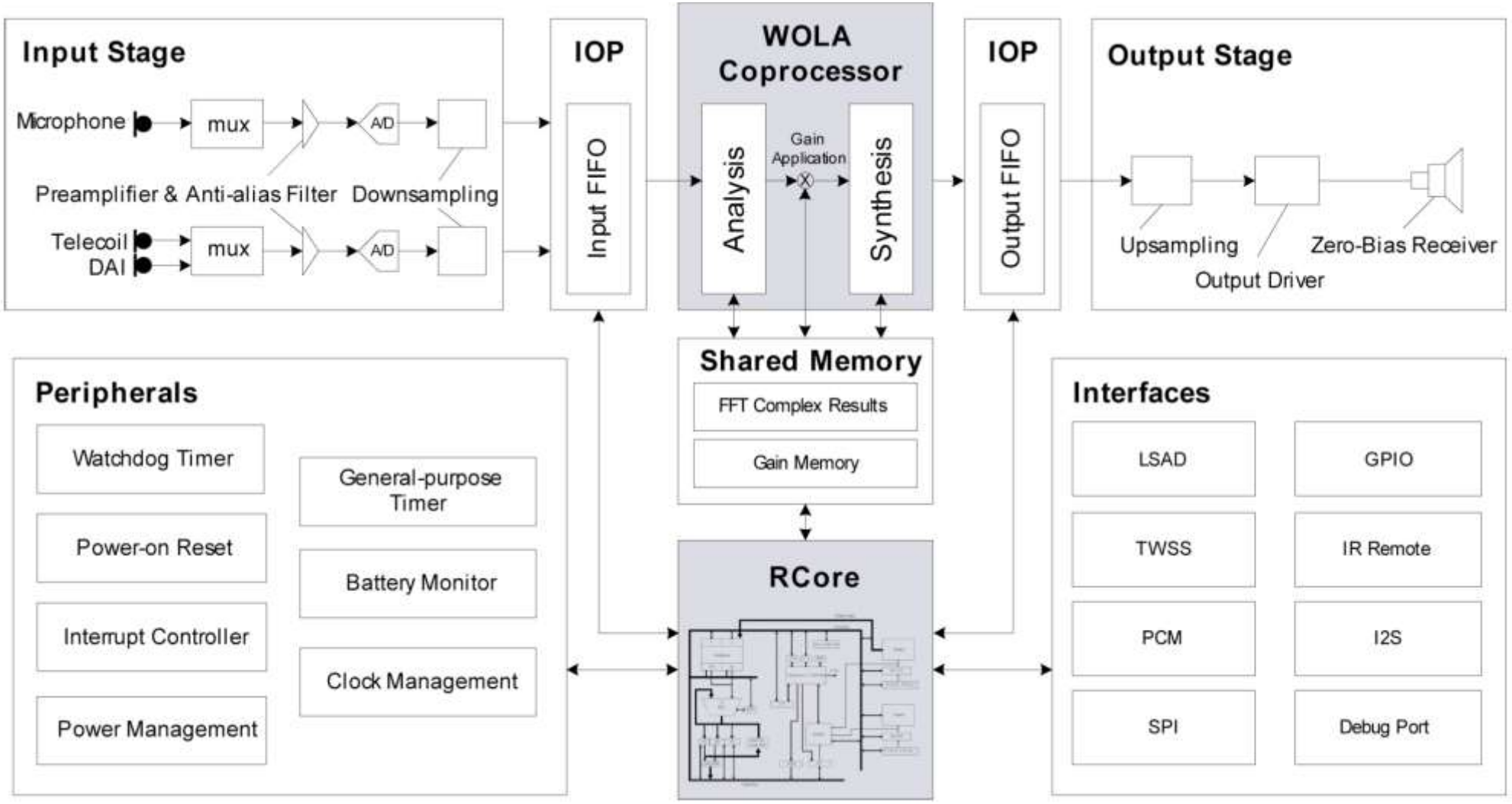
Toccata Plus processor

- dimensions: 5.97 x 3.48 x 1.52 mm (with built-in EEPROM)
- power consumption: 400µA
- system clock frequencies: 1.28MHz, 1.92, 2.56MHz (theoretically from 640kHz to 3.84MHz)
- sampling frequencies up to 40kHz (theoretically up to 60kHz)
- supply voltage: 1.2V
- Built-in WOLA coprocessor (*Weighted Overlap-Add*) responsible for the implementation of Fourier's transformation
- Additional 10-bit LSAD (*Low-Speed Analog-Digital*) converter with typical sampling rate: 1.6kHz
- **Programming only in assembler**

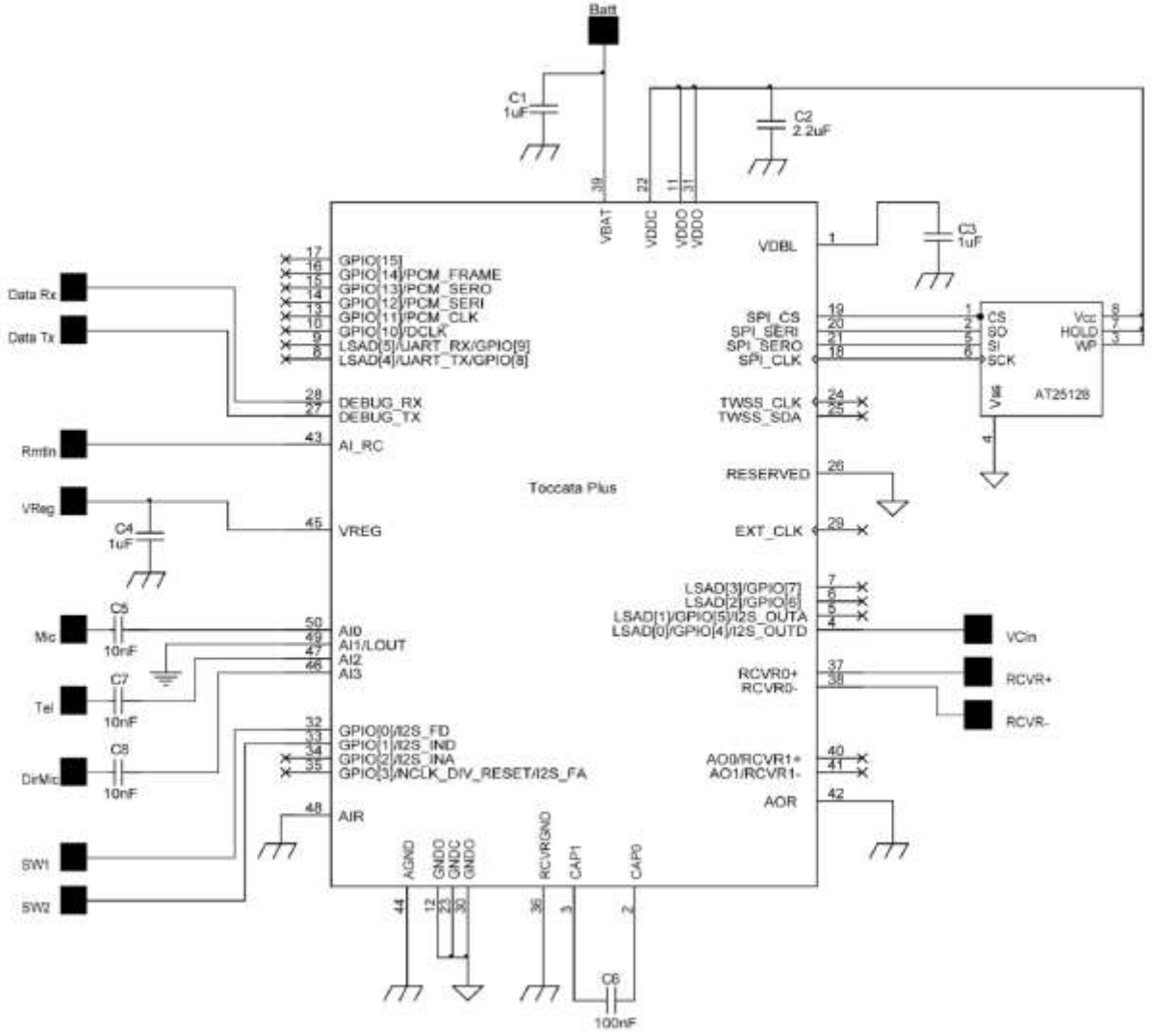
Sampling frequencies

ADC_CTRL_SAMPLE_FREQ	MCLK=640 kHz SYS_CLK= n*MCLK	MCLK=1.28 MHz SYS_CLK= n*MCLK	MCLK=1.92 MHz SYS_CLK= n*MCLK	MCLK=2.56 MHz SYS_CLK= n*MCLK	MCLK=3.84 MHz SYS_CLK= n*MCLK
0x0	10000	20000	30000	40000	60000
0x1	8888.889	17777.78	26666.67	35555.56	53333.33
0x2	8000	16000	24000	32000	48000
0x3	7272.727	14545.45	21818.18	29090.91	43636.36
0x4	6666.667	13333.33	20000	26666.67	40000
0x5	6153.846	12307.69	18461.54	24615.38	36923.08
0x6	5714.286	11428.57	17142.86	22857.14	34285.71
0x7	5333.333	10666.67	16000	21333.33	32000

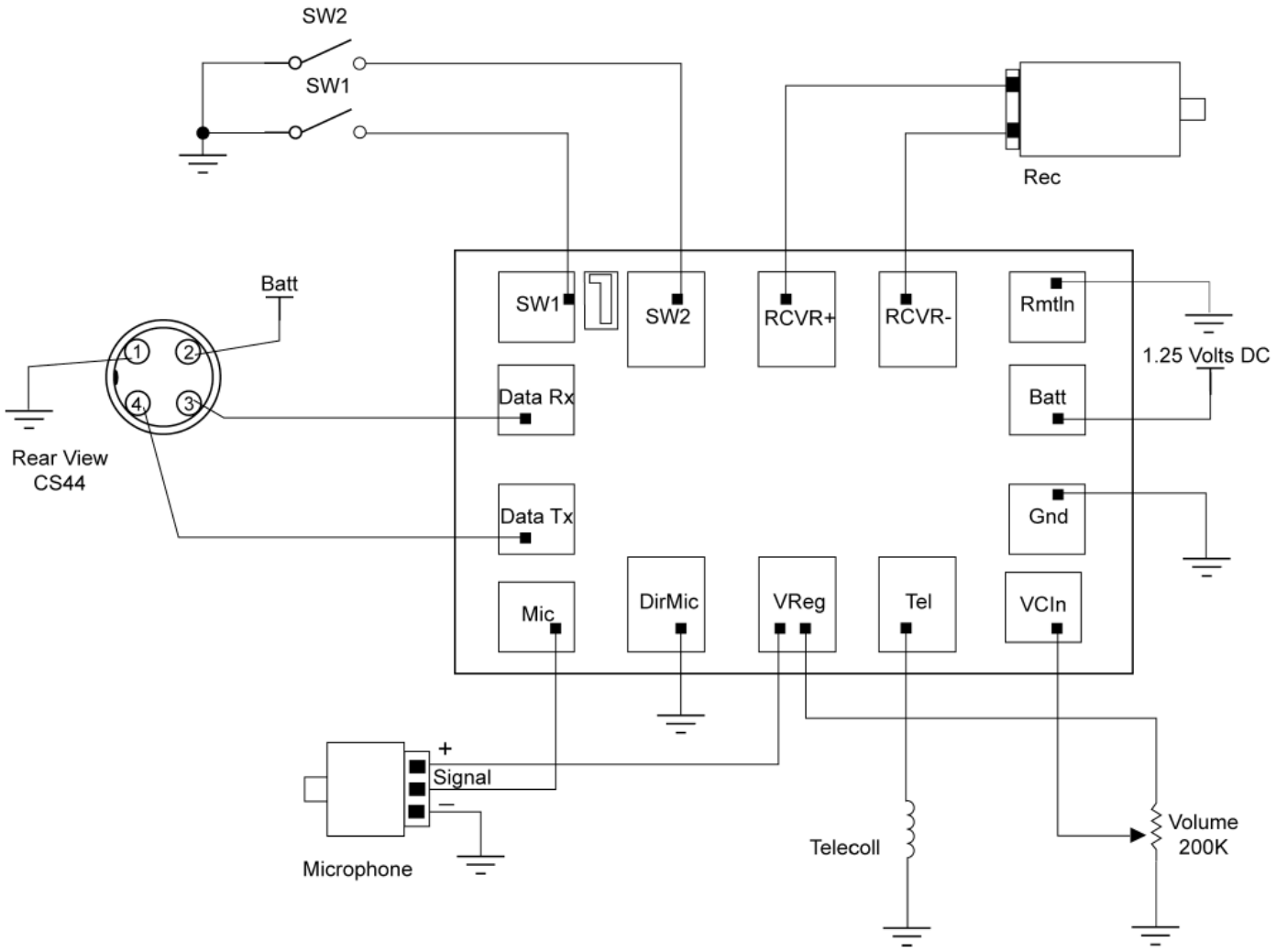
Block diagram



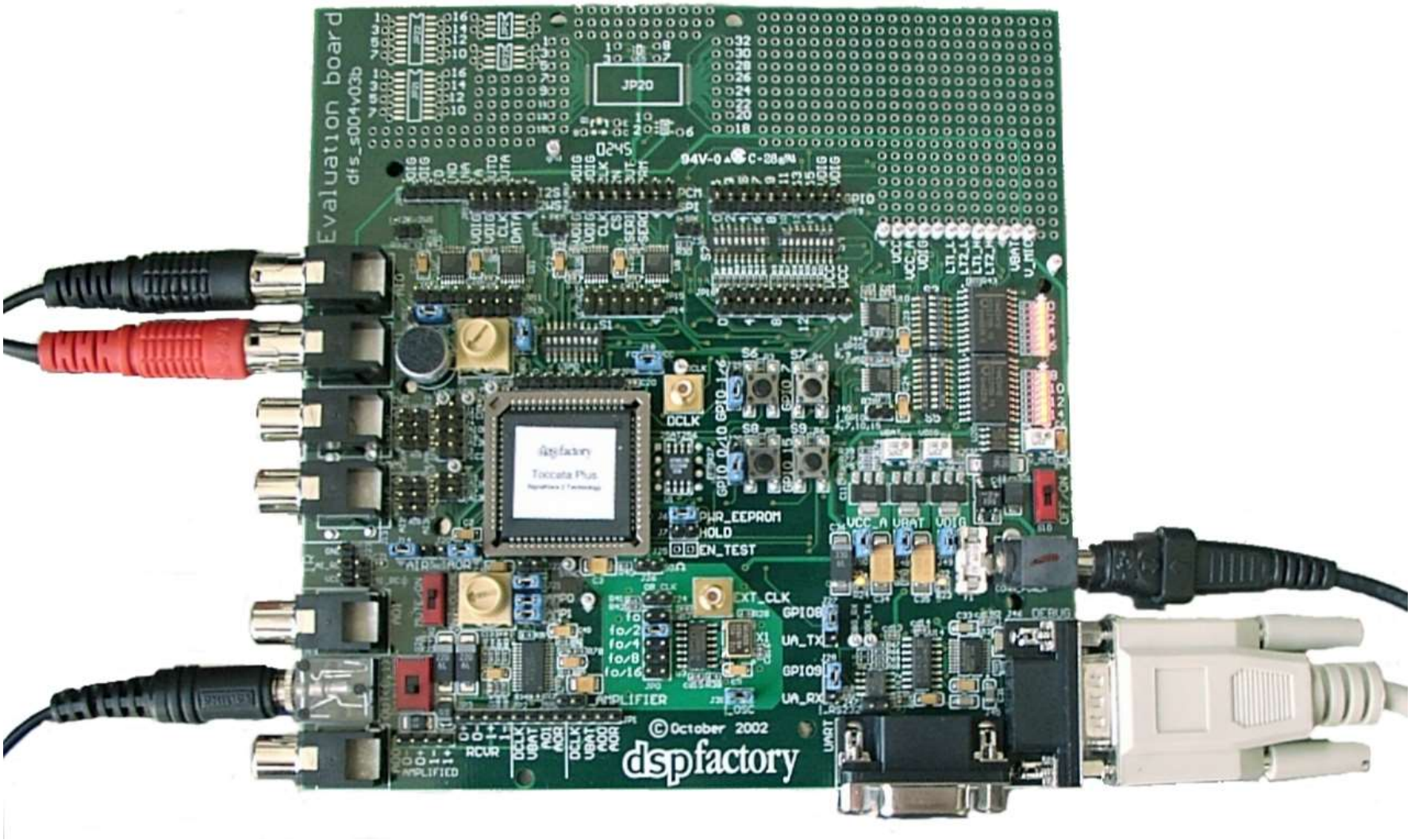
Internal schematic diagram



Typical hearing aid schematic



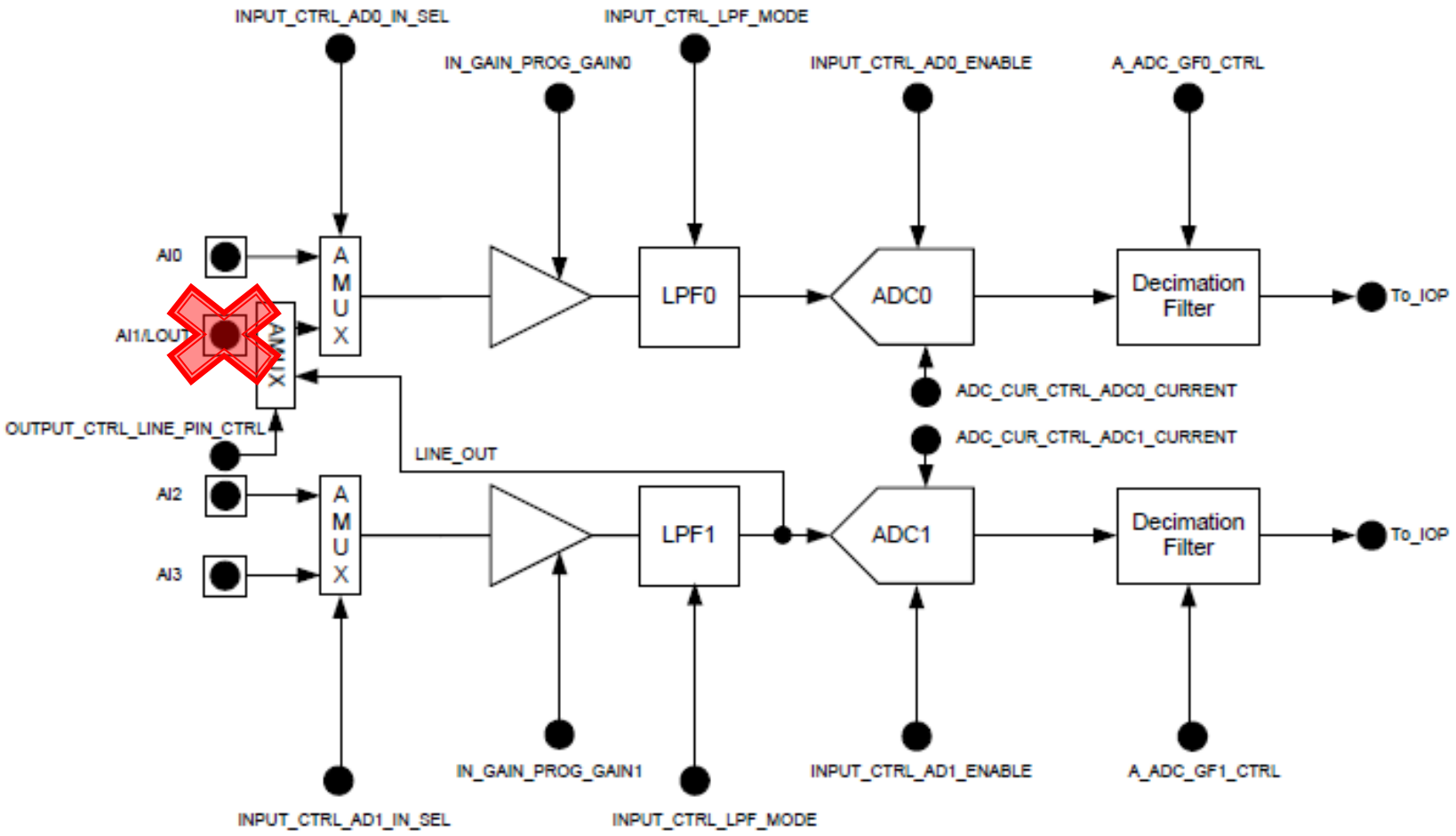
Evaluation board



Input stage

- Two 16-bit sigma-delta oversampling A/D converters
- Two configurable preamplifiers for improved input dynamic range matching
- Two configurable analog 3rd-order anti-aliasing filters
- Two 9th-order low-delay wave digital filters (WDFs) for decimation and DC removal with

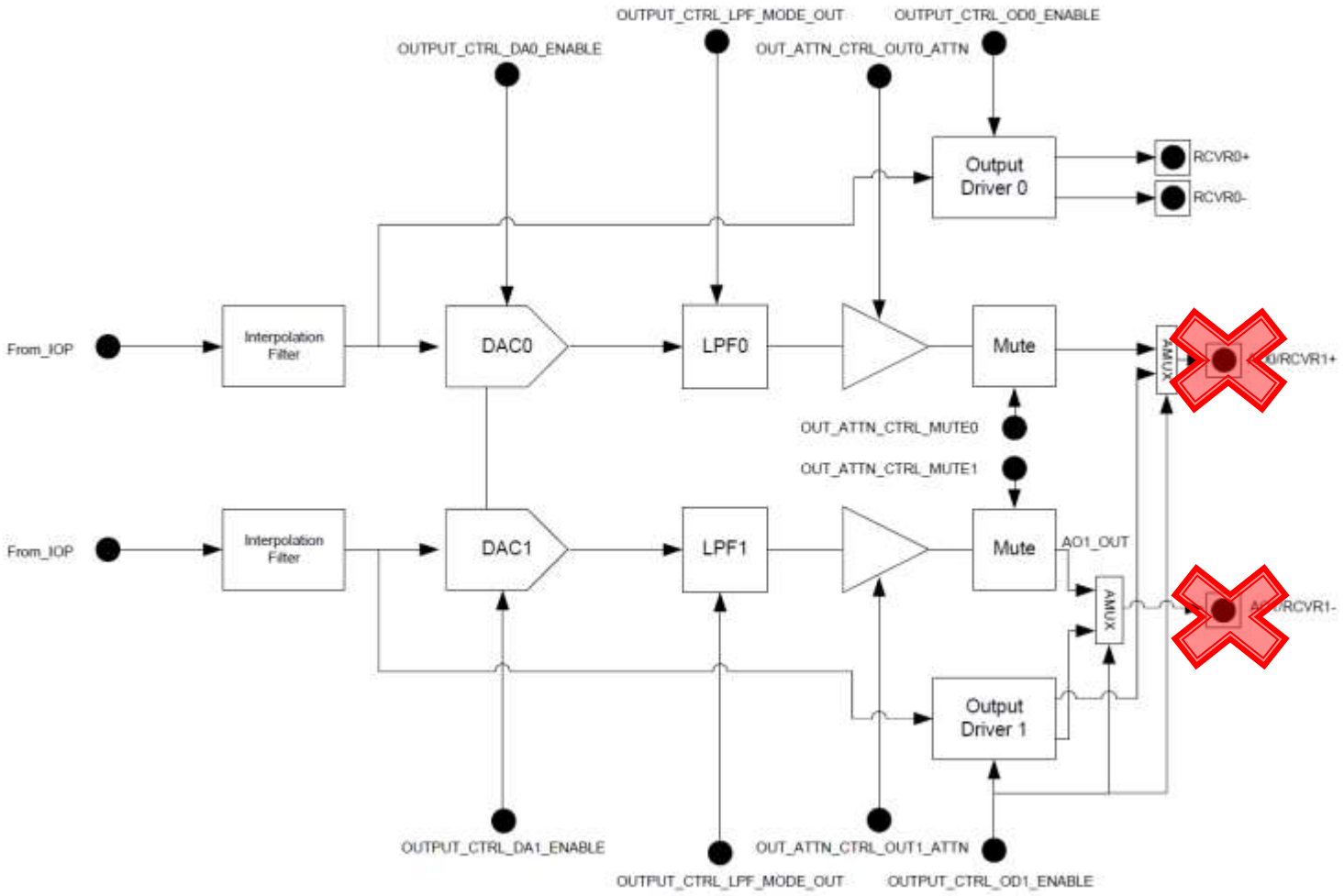
Input stage


INPUT_CTRL_AD0_IN_SEL
INPUT_CTRL_LPF_MODE
IN_GAIN_PROG_GAIN0
INPUT_CTRL_AD0_ENABLE
A_ADC_GF0_CTRL
AI0
AI1/LOUT
AMUX
AMUX
LPF0
ADC0
Decimation Filter
To_IOP
ADC_CUR_CTRL_ADC0_CURRENT
ADC_CUR_CTRL_ADC1_CURRENT
OUTPUT_CTRL_LINE_PIN_CTRL
LINE_OUT
AI2
AI3
AMUX
LPF1
ADC1
Decimation Filter
To_IOP
IN_GAIN_PROG_GAIN1
INPUT_CTRL_AD1_ENABLE
A_ADC_GF1_CTRL
INPUT_CTRL_AD1_IN_SEL
INPUT_CTRL_LPF_MODE

Output stage

- Two 16-bit sigma-delta oversampling D/A converters
- Two analog outputs
- Two configurable output attenuators for improved output dynamic range matching
- Two configurable analog 3rd-order anti-aliasing filters
- Two pulse-density modulation (PDM)-based direct digital drive outputs
  - eliminates the need for additional amplifiers when using passive speakers (receivers)
  - works as a Class D amplifier

Output stage



RCore DSP

- Dual-Harvard architecture, 16-bit programmable fixed-point DSP with three execution units
- A single-cycle multiply-accumulate (MAC) with 40-bit accumulator
- Support for time-domain preprocessing of the input data stream and frequency-domain processing of WOLA output
- Master control functionality for the entire system

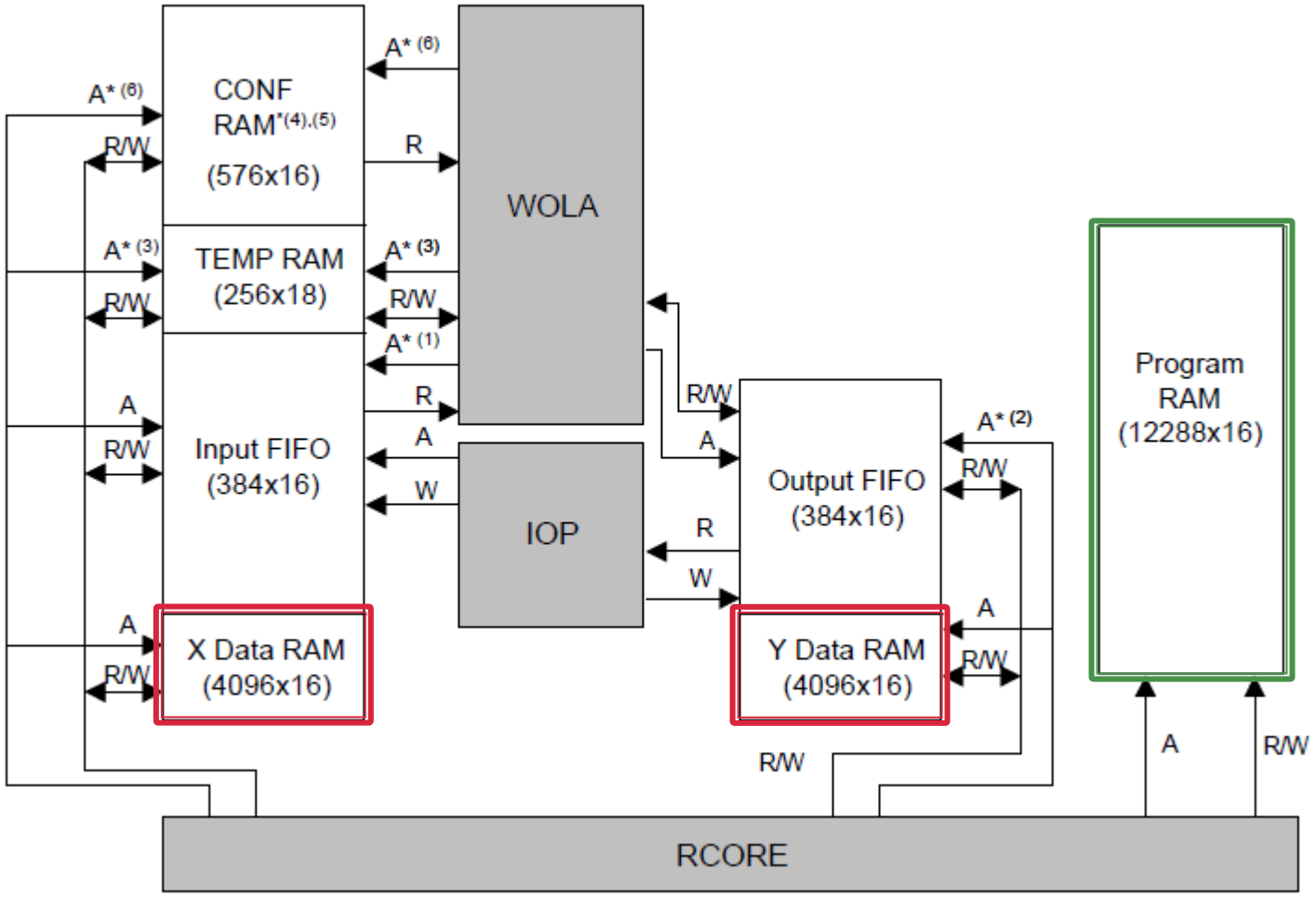
Weighted Overlap-Add (WOLA) filterbank coprocessor

- Block floating-point calculations (2-bit exponent, 16-bit mantissa) to achieve high fidelity
- A standard library of overlap-add (OLA) and weighted overlap-add (WOLA) filterbank configurations:
  - Configurable number of frequency bands
  - Configurable oversampling and decimation factors
  - Configurable windows
- Low group delay (< 4 ms for 16 bands possible)
- Fast real and complex gain application for magnitude and phase processing

IOP Processor

- IOP –Input/Output Processor
  - Block-based DMA for all audio data, for automatic management of input and output FIFOs that reduces processor overhead

Memory Architecture



Frequency domain analysis

- Analysis: converts the time domain data to frequency domain. This function is performed in the WOLA coprocessor.
- Gain calculation: calculates coefficients and parameters based on the generated bands by the analysis filterbank. This function is performed by the RCore processor.
- Gain application: multiplies the input bands by the data calculated from the gain calculation process. It is performed be the WOLA coprocessor.
- Synthesis: converts the modified frequency bands back to the time domain. This function is performed by the WOLA coprocessor.
- The RCore also has access to the time-domain samples before and after a WOLA time-frequency transform and controls the WOLA coprocessor.

Examples of applications

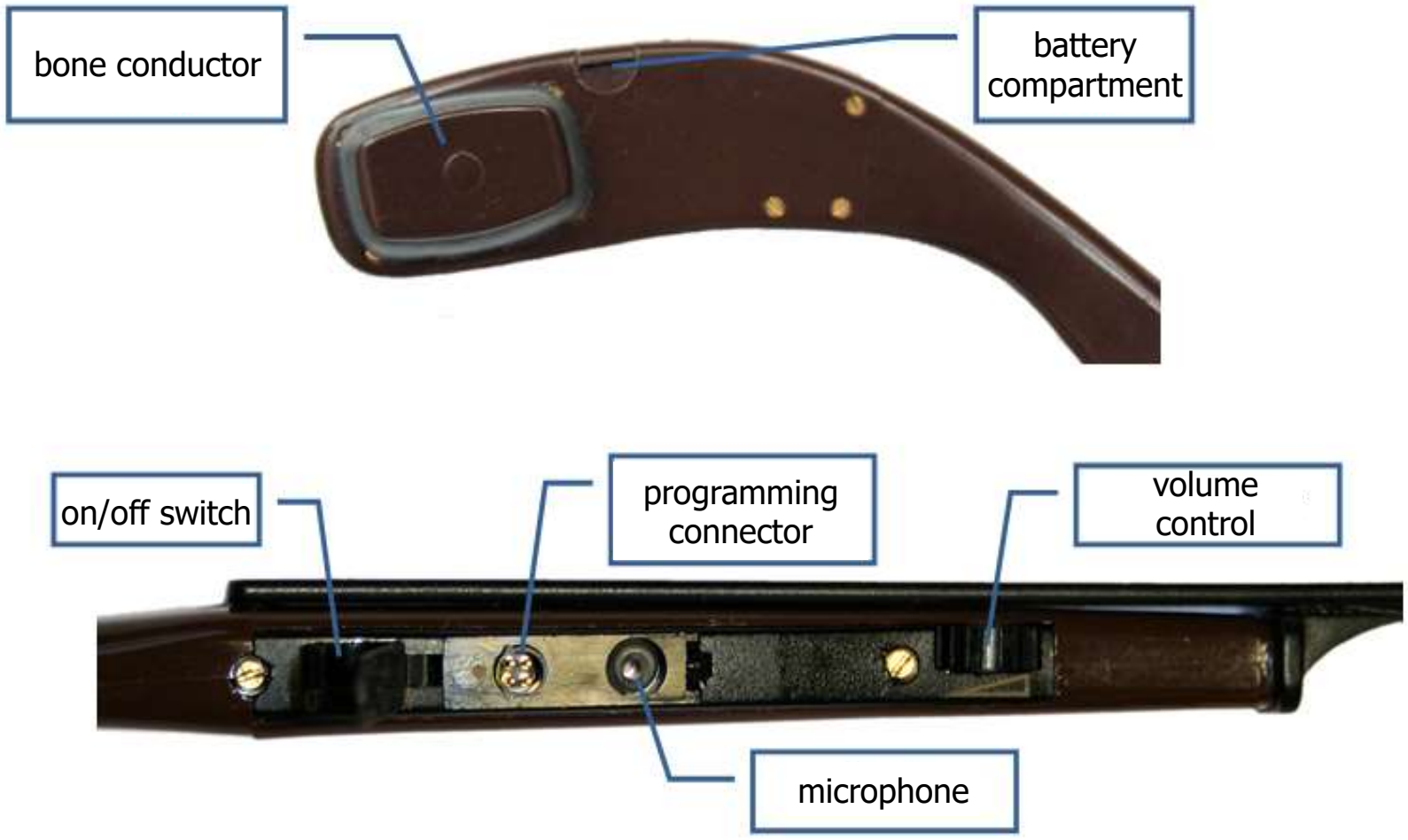
- Hearing aid in a spectacle temple
- Subminiature Digital Speech Aid
- Digital Larynx
- Auditory training

Hearing aid in a spectacle temple

Spectacle frame

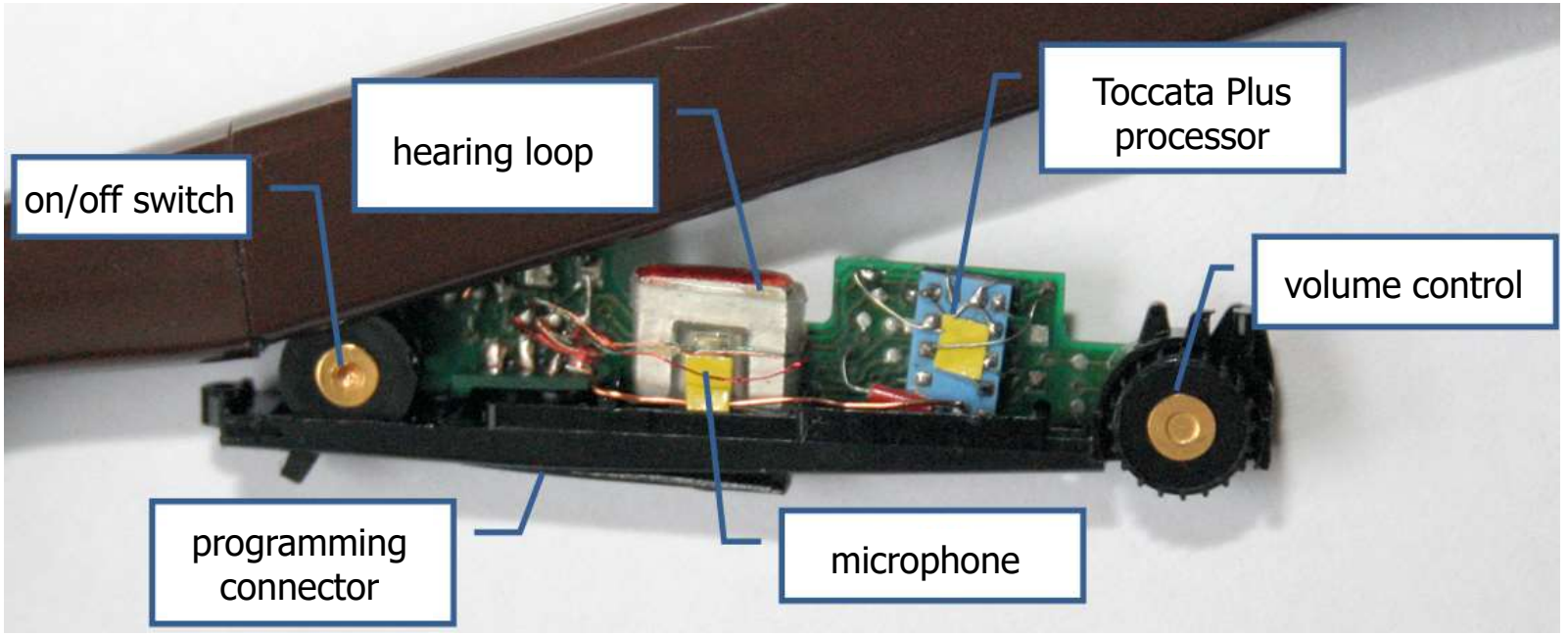
- Complete hearing aid mounted in the spectacle temple: Contact Star EVO1 (BHM company)

Konstrukcja



Problems

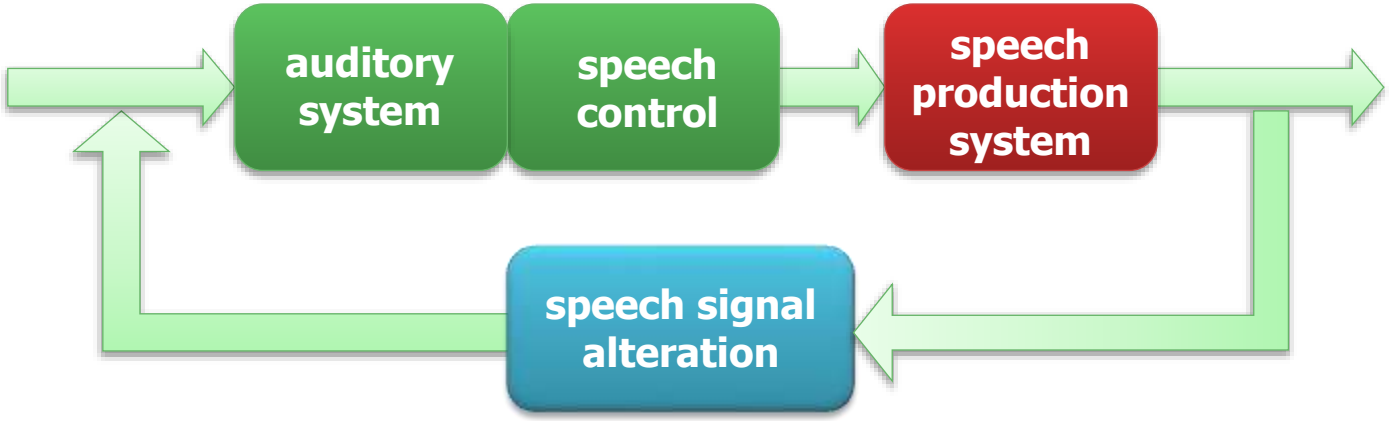
- the manufacturer assumed the use of Gennum Corporation's DSP GA3216 processor
- it was necessary to adapt the electronics of the hearing aid circuit to the Toccata Plus



Subminiature Digital Speech Aid

Stuttering

- the number of stuttering persons ranges from approx. 0.5% to 1% of the population
- conventional therapy methods are not efficient
- the main reason of stuttering are auditory feedback loop disorders
  - change of this loop can help people who stutter



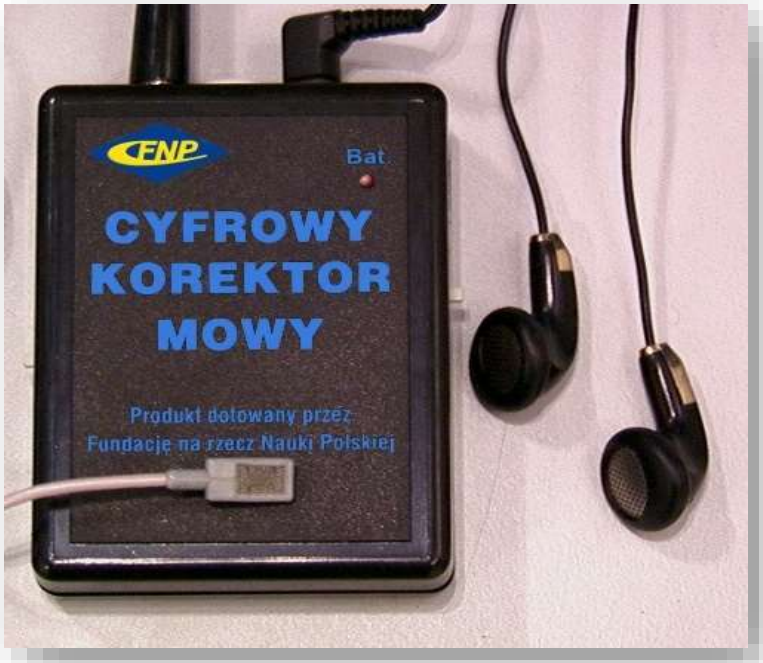
Auditory feedback loop modifications

- it is possible to add modifications in the auditory feedback loop

- MAF – *Masked Auditory Feedback*
- DAF – *Delayed Auditory Feedback*
- FAF – *Frequency Altered Feedback*

Digital Speech Aid (DSA)

- designed at the Gdansk University of Technology in co-operation with the Canadian Dalhousie University
- developed in the early 90s.
- uses DAF and FAF algorithms



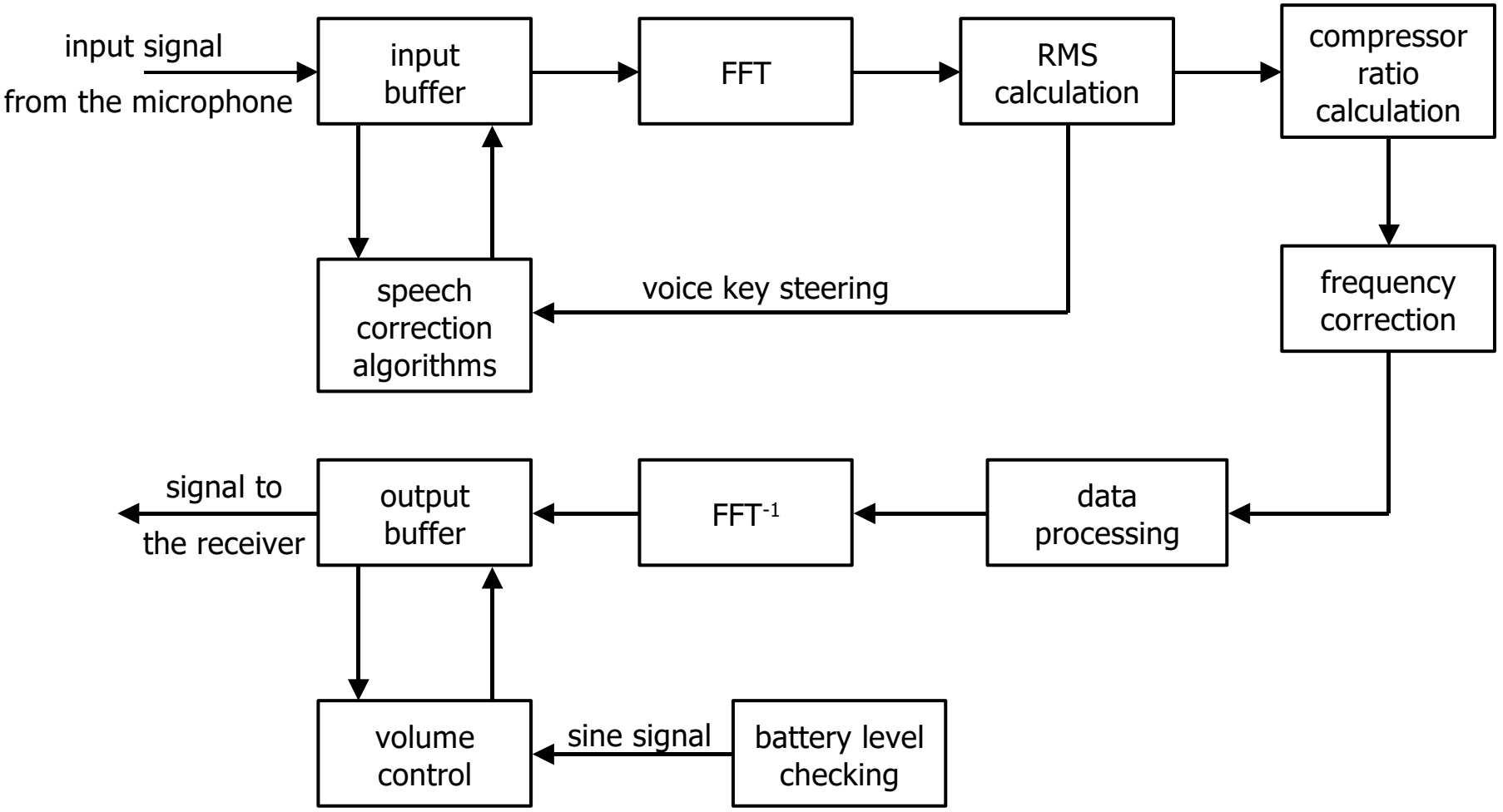
SDSA - assumptions

- the patient uses only one device – in one ear
  - the second ear can receive sounds without processing
- use of common speech correction algorithms: DAF, FAF, DAF+FAF
  - and new, more complex algorithms
- additional algorithms (for sound enhancement)
  - dynamic processing (e.g. compressor)
  - equalizer (16 bands)
  - battery monitor
  - voice key

Subminiature Digital Speech Aid

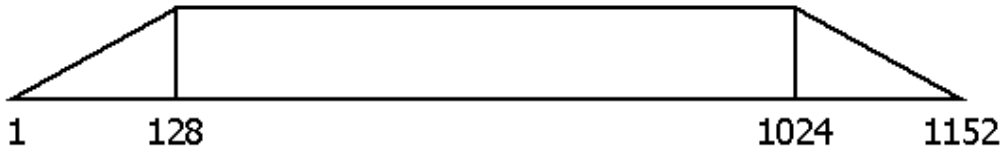
- clock frequency: 1.92MHz;
  - at 1.28MHz, FAF applications worked incorrectly, it was necessary to perform too many calculations in relation to the capabilities of the processor clocked at that frequency
  - sampling rate: 16kHz;
- WOLA processor parameters
  - work on data blocks of 8 samples,
  - the length of the analysis window is 128 samples,
  - FFT length: 32,
  - oversampling and decimation factors equal to 4.

Sound processing



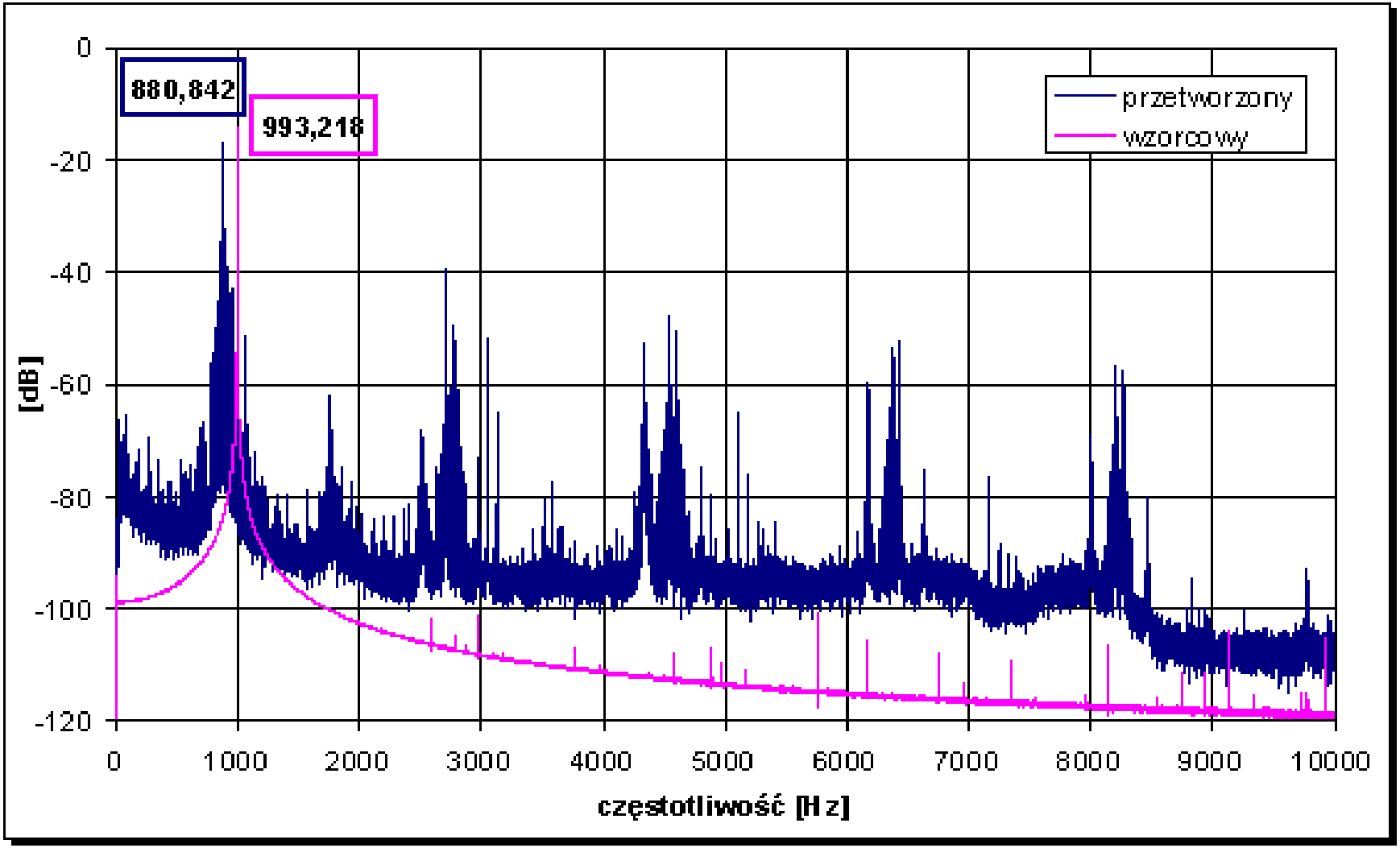
Algorithms

- DAF
  - buffers located in X and Y memory
  - maximum delay: 3200 samples
    - at 16kHz sampl. freq. -> 400ms
- FAF
  - one buffer with two independent indexes (reading and writing) is used
    - it is located in X memory
    - length: 1024 samples



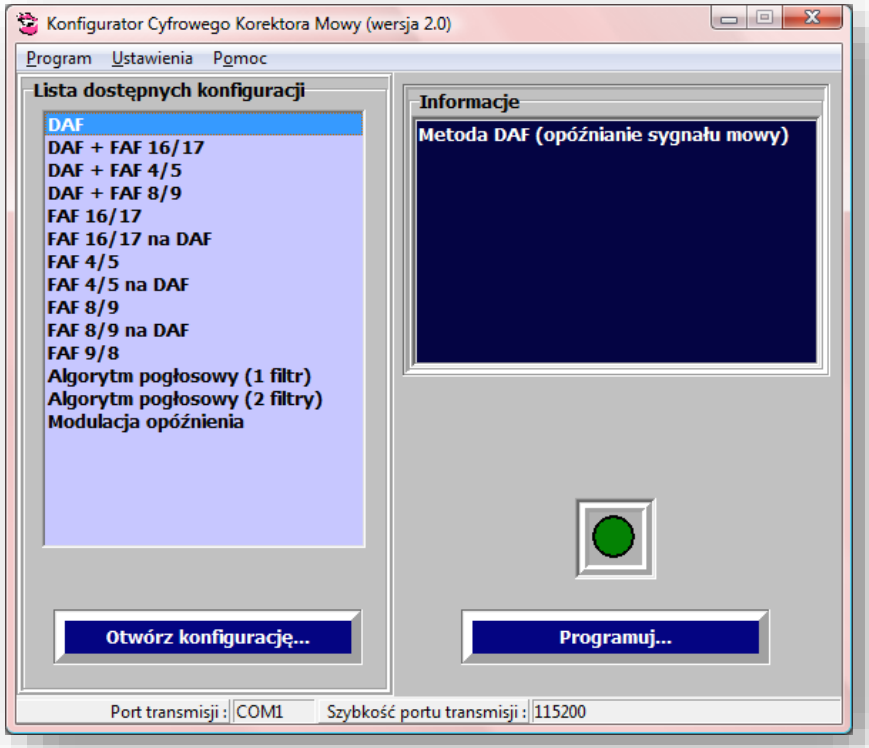
Overlapping example (shift 11% octave)

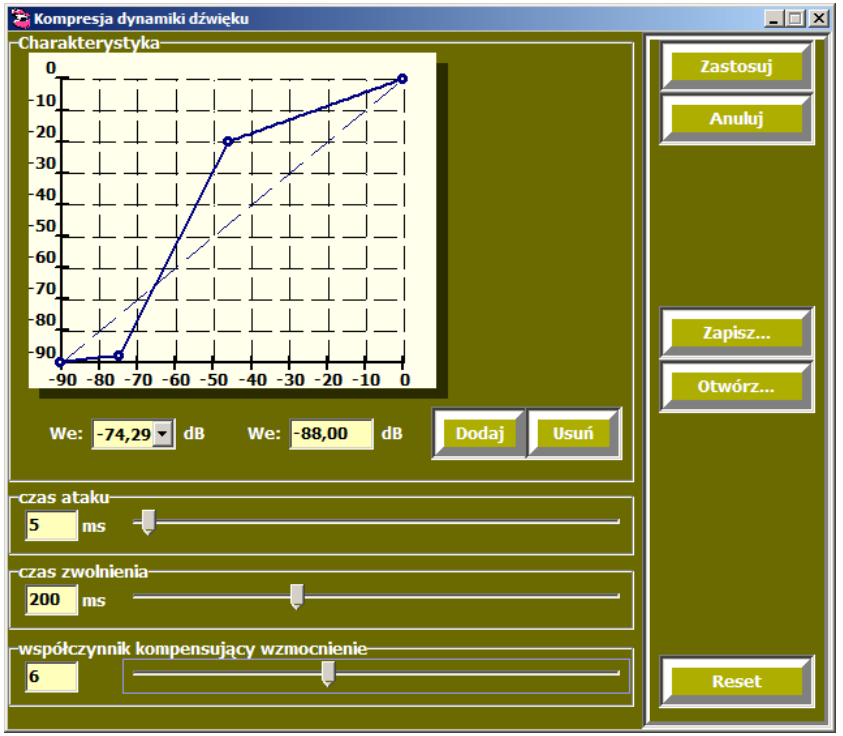
FAF algorithms



PC software

- Algorithms and their parameters can be changed employing special software and hardware
  - presets based on experiments results





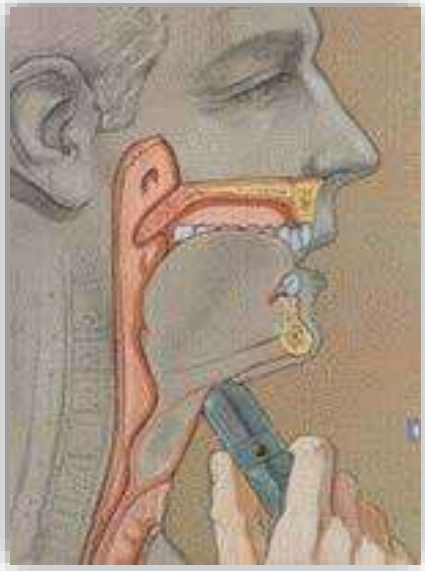
Current consumption

Algorithm	TYPICAL CURRENT CONSUMPTION [μA]	MAXIMUM CURRENT CONSUMPTION [μA]
Modified DAF algorithm (no delay, no additional algorithms, clock frequency 1.28MHz)	200	800
Modified DAF algorithm (no delay, no additional algorithms, clock frequency 1.92MHz)	230	
Modified DAF algorithm (no delay, EQ and dynamic processing, clock frequency 1.92MHz)	310	
Typical DAF algorithm	330	
Typical FAF algorithm	320	
Delay modulation algorithm	330	
Reverberation algorithm	330	

Digital Artificial Larynx (DAL)

Artificial larynx

- produced speech is monotonous and very artificial
- speech intelligibility is poor (about 60%)
- the major problem is a background noise
- construction has been almost unchanged since 1950's

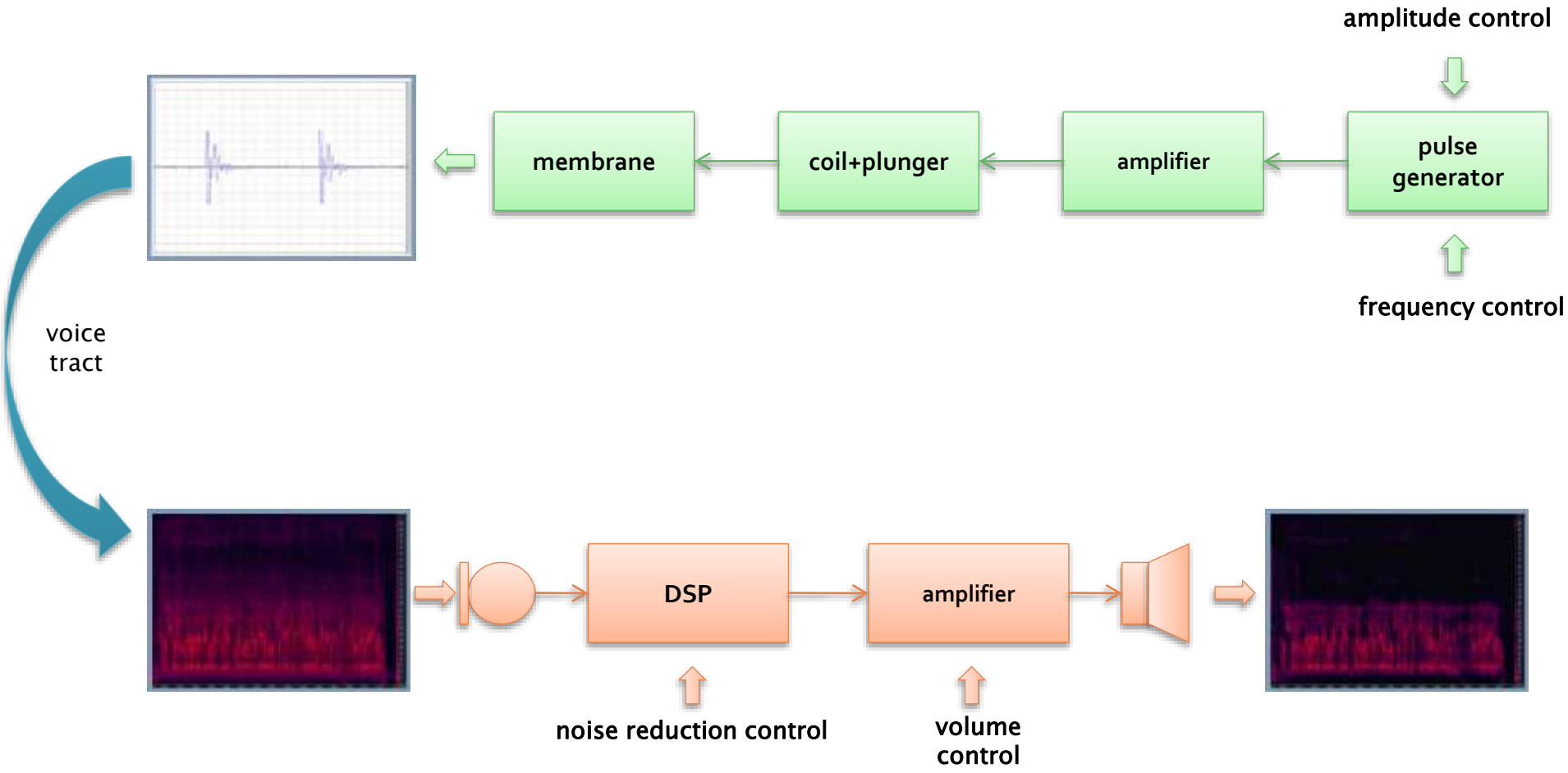


Digital Artificial Larynx

- it is possible to reduce the level of noise and improve the quality of the speech generated by use of digital signal processing

Digital Artificial Larynx

Schemat blokowy:



Spectral subtraction

- **problems**
  - noise and speech signals have the same excitation source and consequently are strongly correlated for voiced sounds
  - noise spectrum has to be estimated from the signal recorded while the speaker keeps his lips closed
  - **patients must keep the lips closed during the first second after the switching the DAL on**

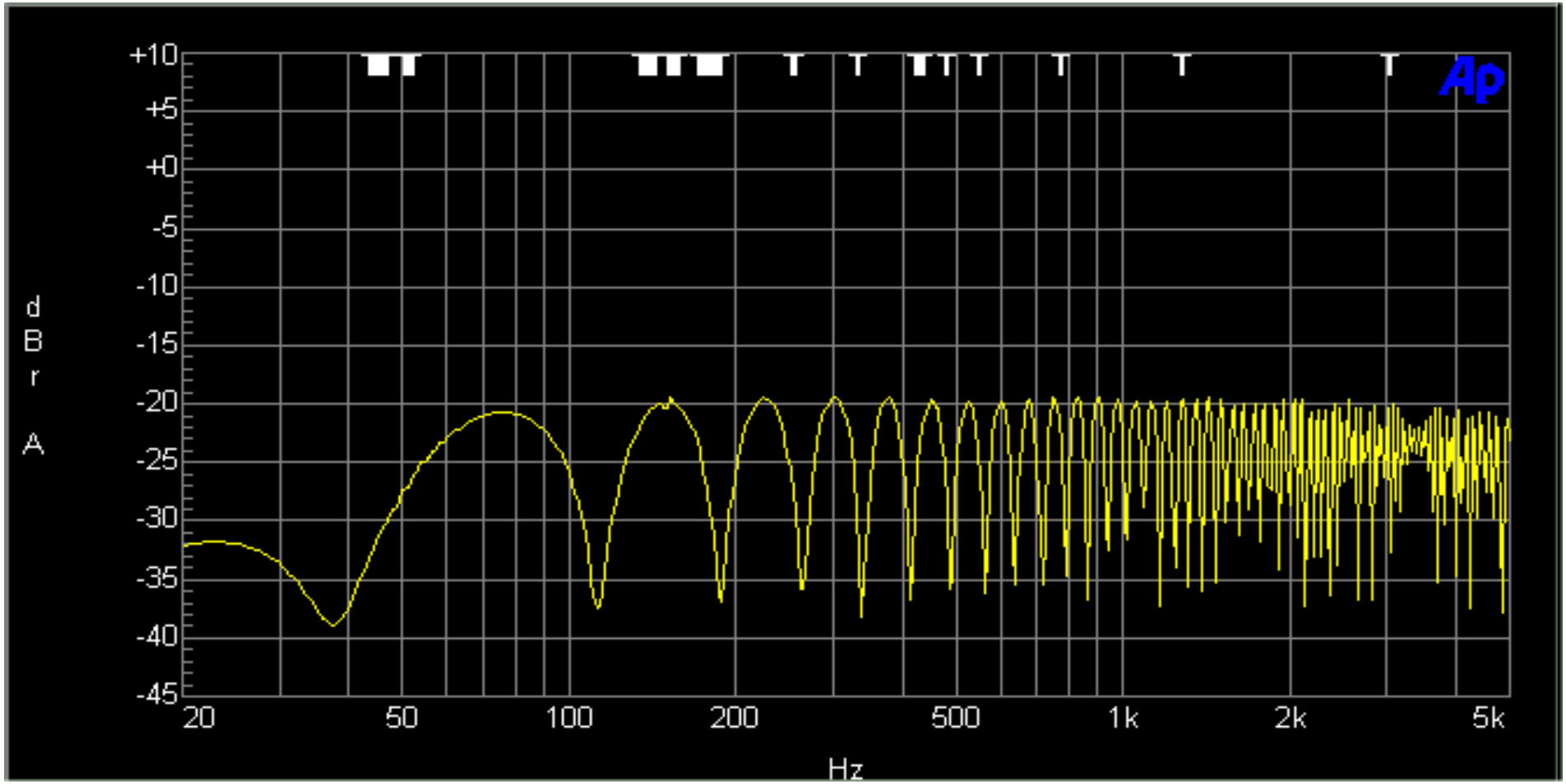
Spectral subtraction

- Parameters of the processor employed are as follows:
  - System clock frequency: 1.28MHz;
  - Sampling frequency: 10.7kHz;
  - Subbands number: 64 (128 points FFT);
  - Frequency resolution is equal to about 83Hz.

Comb Filtering

- less complex algorithm
- spectral characteristic of the filter allows for the precise elimination of maxima of the background noise caused by the device
- main advantage: patient is not required to keep lips closed to obtain the noise sample in order to calculate its spectrum

Comb filtering



Acoustic feedback elimination

- acoustic feedback - serious problem
  - small distance between the microphone and the loudspeaker (about 15-20cm)
- tested solutions
  - notch filter
  - delay modulation
  - spectral transposition

Acoustic feedback elimination

- notch filter
  - impossible to include any adaptive feedback cancellation algorithm
  - insufficient computational efficiency of the employed processor
- delay modulation
  - introduces small changes in the pitch of the produced speech signal
  - modulation signal is a sine wave
  - period of the modulation wave is equal to 1.5 s, average delay is about 30-35 ms and a range of delay changes is set to +/-4 ms
- spectral transposition
  - similar to the FAF (Frequency Altered Feedback) method used in applications for stuttering
  - amount of transposition is set to 6% of octave down the frequency scale

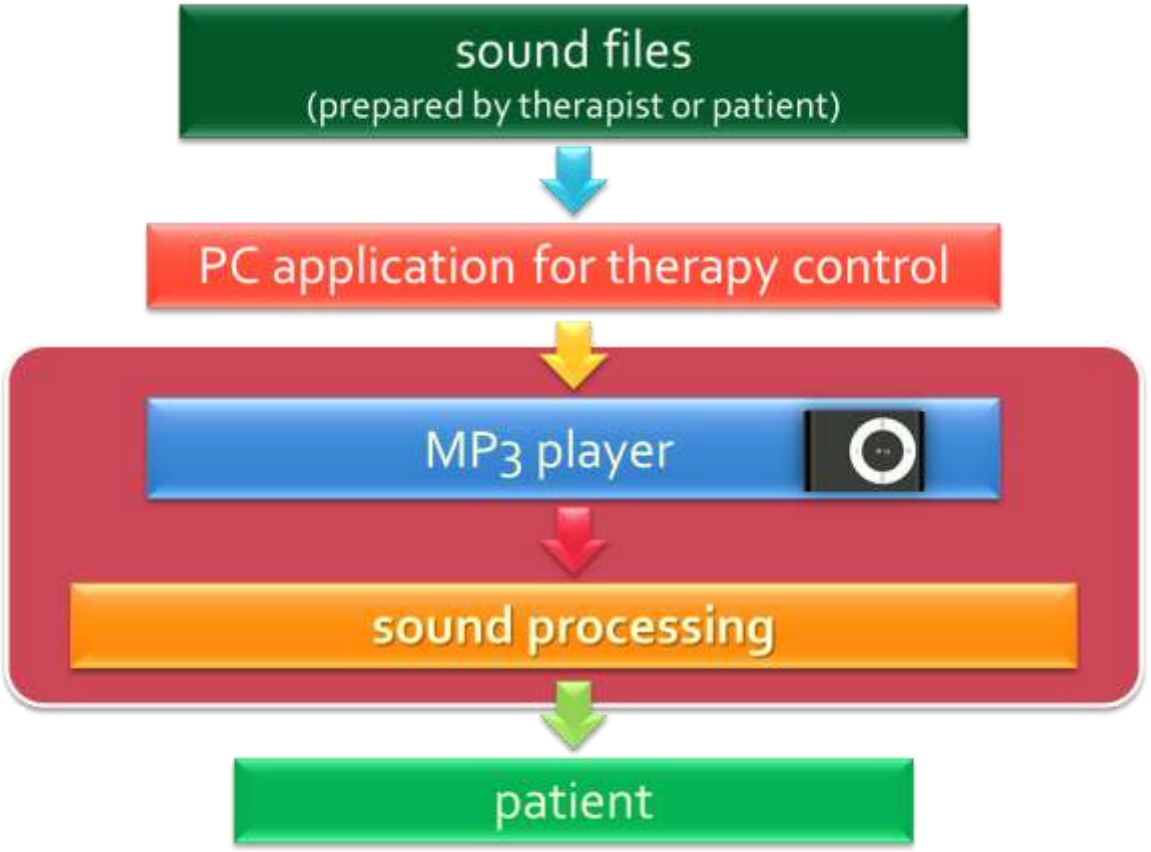
Preliminary tests

- patients were accustomed to speaking immediately after switching the device and in a consequence the speech generated using the spectral subtraction algorithm has bad quality
- patients did not want to use the delay modulation algorithm. Even tough the speech is generated artificially, patients evaluated that it sounded unnaturally to their ears
- the best results were obtained while patients were using the comb filtering algorithm with spectral transposition.

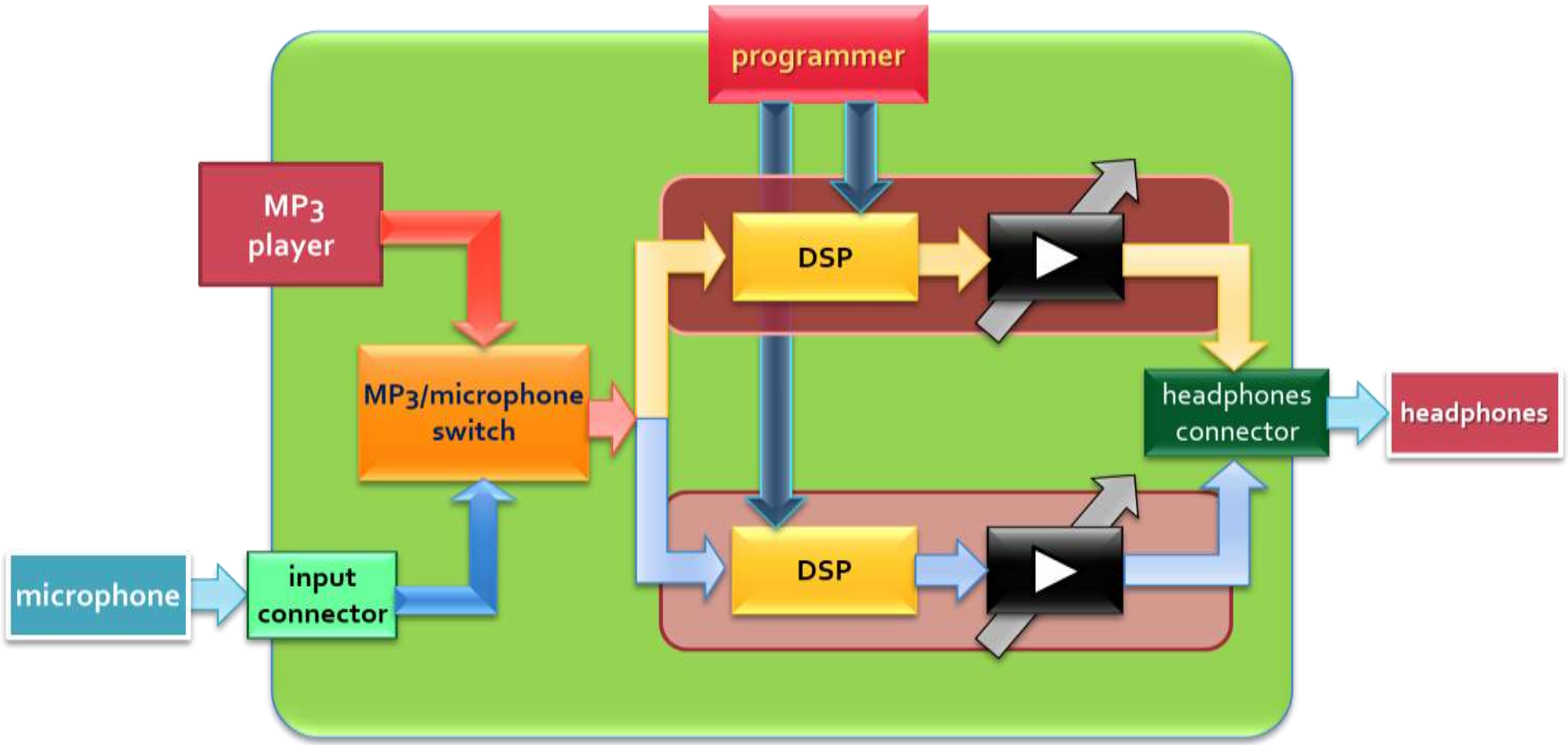
Auditory training

Aim

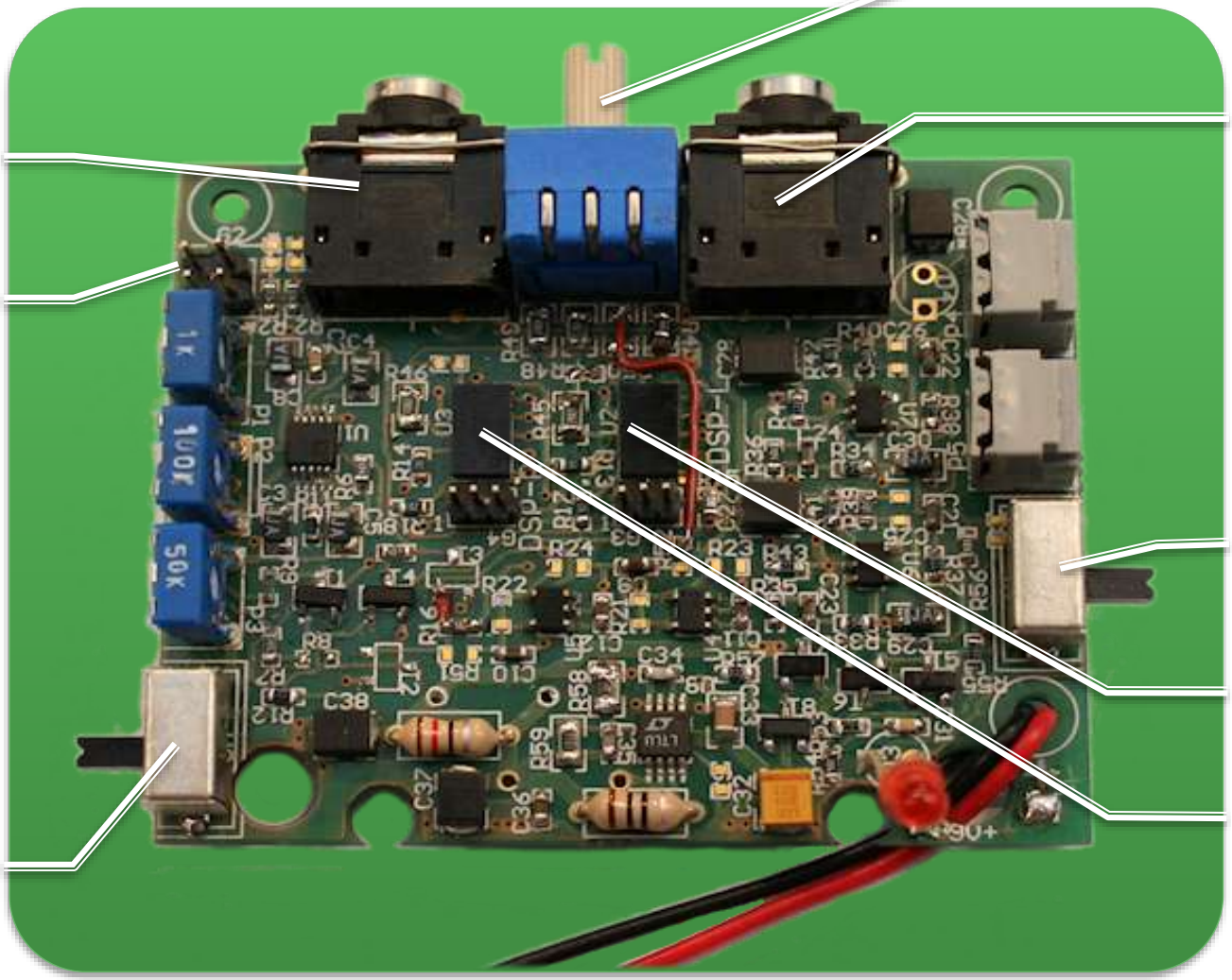
- Development of a small size device that allows the use of various audio processing algorithms



Block diagram



Prototype



programmer

headphone jack

microphone jack

MP3 player input

on/off switch

processor (left channel)

processor (right channel)

MP3/microphone switch

Algorithms

- sound processing algorithms changed by
  - Low-Speed Analog-Digital converter built-in Toccata processor
  - switch (SW2)
- switchable signal source (MP3/microphone)
  - switch SW1

Parameters

- processor
  - system clock frequency: 2,56MHz
  - sampling frequency: 29kHz
  - bandwidth: ok. 14kHz
  - FFT: 32 points

- **current consumption of the entire unit: 2.5mA**

Other solutions

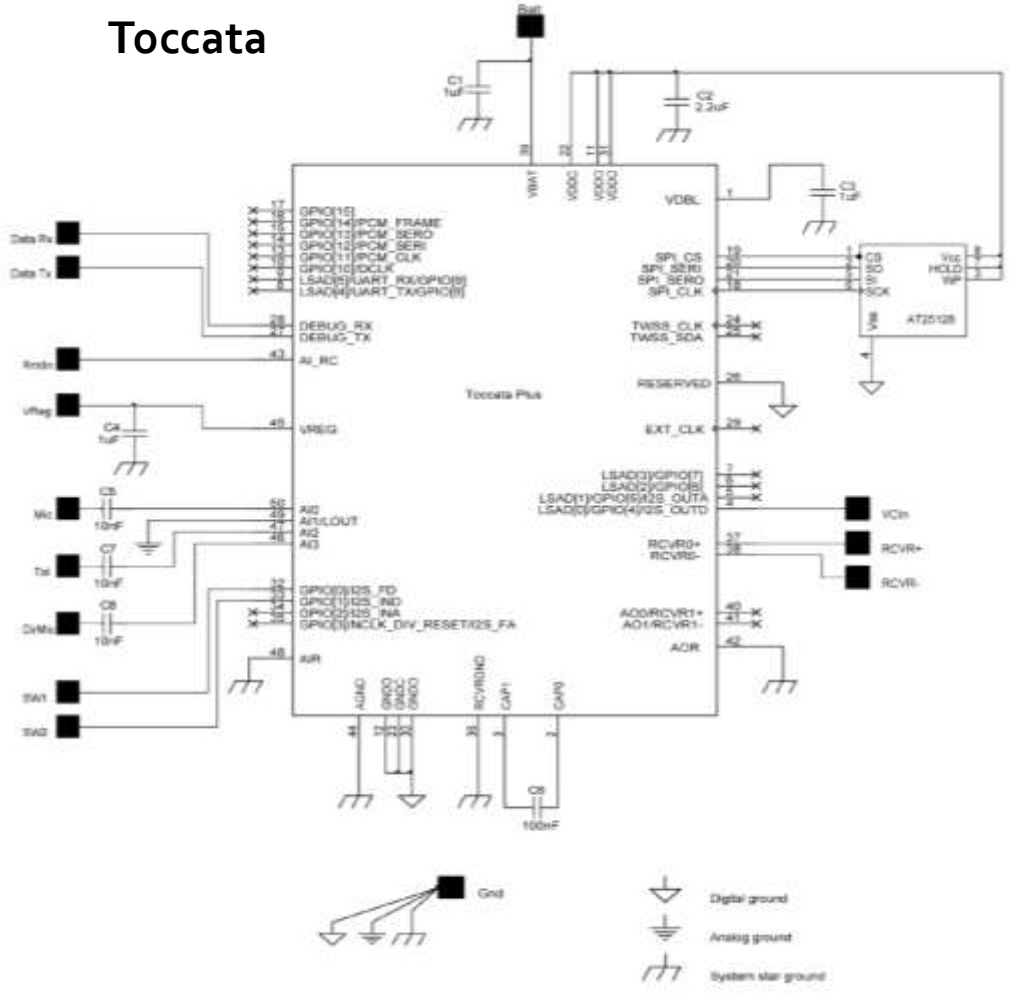
Other processors

- https://www.onsemi.com/products/audio-video-assp/audio-dsp-systems

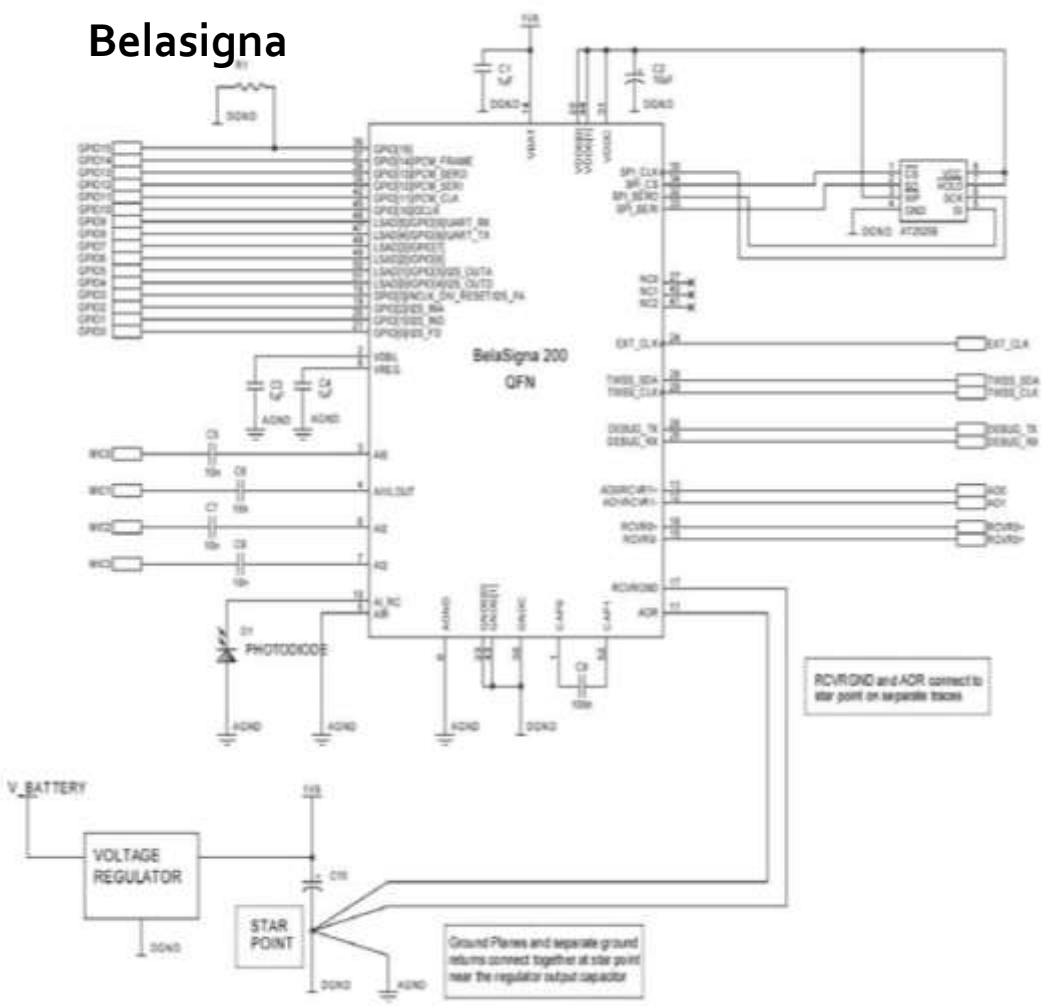
Select	Product	Description	Data Sheet	Pricing ($/Unit) Budgetary price	Compliance	Status	DSP Core (bits)	Coprocessor Type	MIPS	Dynamic Range (dB)	RAM (kB)	Standby Typ (µA)	Audio Inputs	Audio Outputs	Package Type
☐	LC823455	Low Power & High-Resolution Audio Processing System LSI for Portable Sound Solutions		$7.4665		Active	32		170				2	2	WLCSP-120
☐	LC786820E	Compressed Audio Signal Processor IC with USB Host Controller				Product Preview	24	-	64	-	320	-	Analog x3, Digital x3	Analog stereo x1, Analog mono x1, Digital x1	PQFP-100 / QIP-100E
☐	LC786821E	Compressed Audio Signal Processor IC with USB Host Controller and Bluetooth				Product Preview	24	-	96	-	320	-	Analog x3, Digital x3	Analog stereo x1, Analog mono x1, Digital x1	PQFP-100 / QIP-100E
☐	BELASIGNA 200	Single-Chip Audio Processing System				Active	16	WOLA	40	83	42	250	2	2	WLCSP-40
☐	BELASIGNA 300	24 bit Audio Processor for Portable Communication Devices				Active	24	HEAR	-	110	-	60	4	2	WLCSP-35
☐	BELASIGNA R262	Wideband Voice Capture and Noise Reduction SoC				Active	16	WOLA	60	88	-	40	2	2	WLCSP-26
☐	BELASIGNA R281	Always-Listening, Voice Trigger Audio DSP System				Active	16	WOLA	60	-	-	170	1	0	WLCSP-31
☐	FAN3852	Microphone Pre-Amplifier with Digital Output		$0.1733		Active									WLCSP-6
☐	LC703200AW	Speech Processing LSI		$6.5332		Active	32	-	68	88	-	10	2	2	SPQFP-64 / SQFP-64
☐	LC823425	Audio LSI for Portable Sound Solution, Low Power		$10.4904		Active	32	-	110	-	512	-	2	2	LFBGA-221 / FBGA-221J TQFP-128 / TQFP-128L
☐	LC823433TA	Audio Processing System LSI for MP3 Record and Playback Devices				Active	32	-	60	-	246	-	2	2	TQFP-128 / TQFP-128L
☐	LC823450	Low Power & High-Resolution Audio Processing System-on-Chip (SoC)		$10.5997		Active	32	-	160	-	1656	-	2	2	LFBGA240 11x11, 0.65P TQFP-128 / TQFP-128L WLCSP-154

Belasigna 200 processor

Toccata

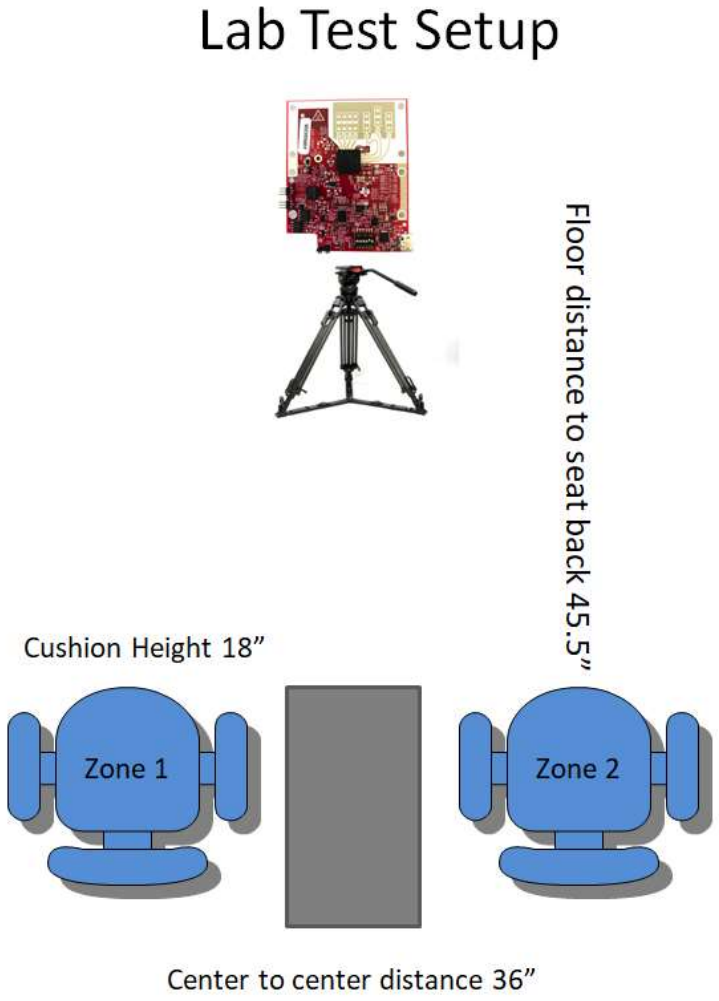


Belasigna



Completely different application

- use of radar sensors to detect people in pre-defined zones of coverage and measure their vital signs such as heart rate and breathing rate



Thank you for attention

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